Mask Set Errata

MSE9S12DT256_4L91N
Rev. 0, 5/2004

Mask Set Errata for MC9S12DT256, Mask 4L91N

MOTOROLA intelligence everywhere™ | digital dna™

Introduction

This mask set errata applies to this MC9S12DT256 MCU mask set:

- 4L91N

MCU Device Mask Set Identification

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 4L91N. All standard devices are marked with a mask set number and a date code.

MCU Device Date Codes

Device markings indicate the week of manufacture and the mask set used. The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code “0201” indicates the first week of the year 2002.

MCU Device Part Number Prefixes

Some MCU samples and devices are marked with an SC, PC, or XC prefix. An SC prefix denotes special/custom device. A PC prefix indicates a prototype device which has undergone basic testing only. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC or SC prefix.

Errata System Tracking Numbers

MUCtsXXXXX is the tracking number for device errata. It can be used with the mask set and date code to identify a specific erratum.

Errata Summary

MUCts00755: BDM

ACK conflict exiting STOP

Description

When using background debug mode to debug code containing STOP instructions, the debugging interface tool can lose clock synchronisation with the MCU target. If the ACK (acknowledge) protocol is enabled, a target command which is expected to send an ACK pulse can conflict with a SYNC (synchronisation) command sent by the debugging interface when attempting to re-establish synchronisation between the interface and the target.

Workaround

The ACK protocol can be disabled when debugging source code which contains STOP instructions. The host SYNC command may then be used to re-establish clock sync between the host and target after a STOP instruction.

MUCts00786: ATD

Write to ATDCTL5 may not clear SCF, CCF and ASCIF flags

Description

If a write to ATDCTL5 happens at exactly the bus cycle when an ongoing conversion sequence ends, the SCF, CCF and (if ASCIE=1) ASCIF flags remain set and are NOT cleared by a write to ATDCTL5.

Workaround

1. Make sure the device is protected from interrupts (temporarily disable interrupts with the I mask bit).
2. Write to ATDCTL5 twice.

MUCts00806: PLL

If osc_clock is 2 to 3 times pll_clock, STOP can cause SCM or reset

Description

This Erratum applies only to systems where PLL is used to divide down the osc_clock by a ratio between 2 and 3. If

1. pll_clock (PLLON=1) is running and
2. 2 < osc_clock ÷ pll_clock < 3 and
3. Full stop mode is entered (STOP instruction with PSTP Bit =0)

there is a small possibility that when entering full stop mode the chip reacts as follows:

1. If self clock mode is disabled (SCME=0) a clock monitor reset will occur. The system does NOT enter full stop mode.
2. If self clock mode and SCM interrupt are enabled (SCME=1 and SCMIE=1) a self clock mode interrupt is generated. The SCMIF flag is set. The system does NOT enter full stop mode.
3. If self clock mode is enabled and SCM interrupt is disabled (SCME=1 and SCMIE=0) the system will enter full stop mode. However, after wakeup, self clock mode is immediately entered without performing the specified clock quality check. The SCMIF flag will be set.

Workaround

1. Avoid osc_clock ÷ pll_clock ratios between 2 and 3.
2. If a osc_clock ÷ pll_clock ratio between 2 and 3 is required, perform the following before entering full stop mode.
   a. Deselect PLL (PLLSEL=0)
   b. Turn off PLL (PLLON=0)
   c. Enter stop
   d. On exit from stop, turn on PLL again (PLLON=1)

MUCts00980: FLASH
STOP instruction may set flash ACCERR flag

Description

If the FCLKDIV flash clock divider register has been loaded, and the flash is not executing a command (flash CCIF command complete flag is set), the execution of a STOP instruction will erroneously set the ACCERR access error bit in the FSTAT flash status register.

Workaround

The ACCERR bit in the FSTAT register must be cleared after the execution of a STOP instruction if the FCLKDIV register has been loaded.

MUCts00987: EEPROM
STOP instruction may set EEPROM ACCERR flag

Description

If the ECLKDIV EEPROM clock divider register has been loaded, and the EEPROM is not executing a command (EEPROM CCIF command complete flag is set), the execution of a STOP instruction will erroneously set the ACCERR access error bit in the ESTAT EEPROM status register.

Workaround The ACCERR bit in the ESTAT register must be cleared after the execution of a STOP instruction if the ECLKDIV register has been loaded.

MUCts01011: ECT

Input pulse shorter than delay counter period recognised as valid

Description An input capture pulse whose pulse width is shorter than delay counter window is erroneously recognized as a valid pulse. The MCU interrupt flags will be set and an ISR will be called if the IRQ is enabled. The interrupt service routine will be delayed by the time set in the delay counter control register. This erratum only affects ECT channels 0 to 3.

Workaround User software should check the logic level of the input capture pin within the interrupt service routine and compare this with the logic level when the input is not asserted. This can be performed using the appropriate registers in the port integration module.

If the pin reads the logic level of the inactive state, the pulse is shorter than the time defined in the delay counter control register plus the interrupt latency. In this case, the pulse triggering the input capture is not valid (too short), hence the interrupt can be acknowledged and exited without further action taking place. If the pin reads the logic level of the active state, the input pulse is valid and the interrupt should be acknowledged and the correct input capture service routine executed.

The effectiveness of this workaround must be evaluated by identifying the worst case latency involved in the call of the ISR. To maximise the effectiveness of pulse rejection, users must consider checking the value in the capture register against the free-running timer on every new capture.

MUCts01026: ATD

CCF flags in ATDSTAT1 register might fail to set

Description The setting of the CCF7-0 flags in ATDSTAT1 register is not independent of the clearing. A clear on CCFx (e.g. Bit AFFC=1 and read of ATDDRx) which occurs in exactly the same bus cycle as the setting of any other flag CCFy (x,y = 0,1,..,7; x!=y) masks the setting of CCFy. CCFy will not set in this special case although the corresponding conversion has completed and the result (ATDDRy) is valid.

Workaround None

MUCts01028: ATD

Clearing of CCF flags in ATDSTAT2/1 by write of ATDCTL5 might not work

Description

Starting a new conversion by writing to the ATDCTL5 register should clear all CCF flags in the ATDSTAT2/1 registers. This does not always work if the write to ATDCTL5 register occurs near the end of an ongoing conversion. Although all CCF flags are cleared one CCF flag might be set again within the 1st ATD clock period of the new conversion.

Workaround

If the unexpected setting of one CCF flag can not be accepted by the application one of the following workarounds can be taken:

1. Abort conversion (e.g. by write to ATDCTL3)
   Pause for 2 ATD clock periods
   Start new conversion
2. Ignore first conversion sequence and clear CCF flags

MUCts01046: EEPROM

Cumulative EEPROM W/E Cycle Limit For 'V' & 'M' Rated Products

Description

Note: This erratum only affects 'V' (105ºC) and 'M' (125ºC) temperature rated products. 'C' temperature rated (85ºC) products are NOT affected.

The EEPROM charge pump durablility limits the cumulative number of sector program/erase cycles at operating temperatures greater than or equal to 105ºC ambient. A program/erase cycle is defined as an erase operation on a sector followed by two program operations, one on each word of the sector. EEPROM program/erase cycling is bound by the following criteria:

1. Any single byte or sector is limited to a certain number of program/erase cycles as detailed in the following table:

		Min	Typ	Max	
EEPROM number of Program/Erase cycles: ($-40ºC \le T_j \le 0ºC$)	n_{EEPE}	10,000			Cycles
EEPROM number of Program/Erase cycles: ($0ºC \le T_j \le 140ºC$)	n_{EEPE}	100,000			Cycles

2. The cumulative number of sector program/erase cycles is bound as

detailed in the table below:

			Min	Typ	Max	
Number of EEPROM sector cumulative program/erase cycles	125ºC (M) 105ºC (V) 85ºC (C)	n_{MAX}	20.0M 30.0M 102.4M(1)			Cycles

1. Note that 102.4M sector cycles is equivalent to 100,000 full array (4096 bytes = 1024 sectors) cycles as commonly specified.

The charge pump durability imposes a limit on the cumulative number of program/erase cycles. However, any particular area of the EEPROM array has high (up to 100k) program/erase cycle endurance capability at elevated temperatures as demonstrated and bound in the following example:

Example

The MC9S12DT256 EEPROM module has 1024 EEPROM sectors (1 sector = 4 bytes).

Definitions:

n = Number of areas of EEPROM.

X = Number of sectors in an area of EEPROM. In this example X = 1024 sectors.

Y = Number of program/erase cycles for all X sectors in the area . In this example Y = 100k cycles (0ºC = Tj = 140ºC).

X*Y = Cumulative number of program/erase cycles possible across X sectors in the particular area.

'C' Rated Product (85ºC Temperature):

Capability: Full specification.

1024 sectors (full array (n = 1)) x 100k cycles = 102.4M cumulative program/erase cycles are possible.

'V' and 'M' Rated Product (105ºC & 125ºC Temperature):

Capability: Reduced cumulative number of program/erase cycles.

125ºC: $\sum_{i=1}^{n} Xi \times Yi \leq$ 20M cumulative program/erase cycles are possible.

105ºC: $\sum_{i=1}^{n} Xi \times Yi \leq$ 30M cumulative program/erase cycles are possible.

Application Based Example

To evaluate the impact on a particular application, an understanding of the specific use of the EEPROM array is necessary. For example, consider an application running on an MC9S12DT256 device which requires maximum endurance (100k cycles) from 128 sectors (one eighth of the EEPROM array - area 1), high endurance (25k cycles) from 256 sectors (one quarter of the EEPROM array - area 2) and the remaining 640 sectors (area 3) are program/erase cycled infrequently (1000 cycles). The following is an example calculation for total cumulative cycles at maximum continuous operating temperature (125ºC):

From specification above @ 125ºC:

$$\sum_{i=1}^{n} Xi \times Yi \leq 20M$$ cumulative program/erase cycles are possible.

Area 1 Area 2 Area 3

$$(128\text{Sectors} \times 100\text{kCycles}) + (256\text{Sectors} \times 25\text{kCycles}) + (640\text{Sectors} \times 1000\text{Cycles}) = 19.84\text{MCycles}$$

This calculation shows that this particular application will not be affected by this erratum because the maximum number of cycles over the MCU lifetime will not exceed the new specification limit.

Workaround None

MUCts01104: MSCAN
Time stamp corrupted in receive buffer

Description When the foreground receive buffer (RxFG) is read, with the Receiver Full Flag (RXF) set, the value of the Time Stamp Register may be incorrect due to corruption. The Time Stamp Register is written correctly when the message is received, but may be overwritten by the timer value at the end of a subsequent reception. The corruption can only occur close to a data overrun, when the receive buffer FIFO is full. The problem occurs whenever the following two conditions are met:

1. Receive buffer system is full. All five receive buffers contain valid

messages waiting to be read by the application.

2. Another valid message is seen on the bus. This message must be sent from another node, i.e. it must not be transmitted from the respective msCAN module itself. At the end of the message in 2. the Time Stamp Register of the oldest message in the receive FIFO is overwritten.

NOTE: *If the message in 2. passes the message filter system the Overrun Interrupt Flag (OVRIF) is also set.*

Workaround

The application software has to ensure to read the receive messages in due time to avoid data overrun in any case. This will automatically minimize the risk of a Time Stamp Register overwrite event.

HOW TO REACH US:

USA/EUROPE/LOCATIONS NOT LISTED:

Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217
1-303-675-2140 or 1-800-441-2447

JAPAN:

Motorola Japan Ltd.; SPS, Technical Information Center,
3-20-1, Minami-Azabu Minato-ku, Tokyo 106-8573 Japan
81-3-3440-3569

ASIA/PACIFIC:

Motorola Semiconductors H.K. Ltd.;
Silicon Harbour Centre, 2 Dai King Street,
Tai Po Industrial Estate, Tai Po, N.T., Hong Kong
852-26668334

TECHNICAL INFORMATION CENTER:

1-800-521-6274

HOME PAGE:

http://www.motorola.com/semiconductors

MOTOROLA