

## FEATURES

### Initial accuracy

**A grade:  $\pm 0.70\%$  (maximum)**

**B grade:  $\pm 0.35\%$  (maximum)**

### Maximum temperature coefficient

**A grade: 50 ppm/ $^{\circ}\text{C}$**

**B grade: 25 ppm/ $^{\circ}\text{C}$**

**$C_{\text{LOAD}} = 0.1 \mu\text{F}$  to  $1 \mu\text{F}$**

**Output current: +4 mA/–2 mA**

**Low operating current: 80  $\mu\text{A}$  (typical)**

**Output noise: 6  $\mu\text{V}$  p-p at 1.0 V output**

**Input range: 2.0 V to 18 V**

**Temperature range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$**

**Tiny, Pb-free TSOT package**

## APPLICATIONS

**Battery-powered instrumentation**

**Portable medical equipment**

**Communication infrastructure equipment**

## GENERAL DESCRIPTION

The **ADR130** is the first family of tiny, micropower, low voltage, high precision voltage references in the industry. Featuring 0.35% initial accuracy and 25 ppm/ $^{\circ}\text{C}$  of temperature drift in the tiny TSOT-23 package, the **ADR130** voltage reference only requires 80  $\mu\text{A}$  for typical operation. The **ADR130** design includes a proprietary temperature drift curvature correction technique that minimizes the nonlinearities in the output voltage vs. temperature characteristics.

## PIN CONFIGURATION

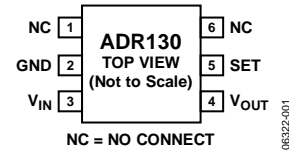


Figure 1. 6-Lead TSOT (UJ-6)

Available in the industrial temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , the **ADR130** is housed in a tiny TSOT package.

For 0.5 V output, tie SET (Pin 5) to  $V_{\text{OUT}}$  (Pin 4). For 1.0 V output, tie SET (Pin 5) to GND (Pin 2).

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**REVISION HISTORY**

**8/2018—Rev. C to Rev. D**

Change to General Description Section ..... 1  
 Change to Specified Temperature Range Parameter, Table 3 ..... 5  
 Added Junction Temperature Range Parameter, Table 3 ..... 5  
 Changes to Ordering Guide ..... 15

**3/2013—Rev. B to Rev. C**

Changes to Figure 34 and Figure 35..... 13

**11/2011—Rev. A to Rev. B**

Change to  $C_{LOAD}$  in Features Section..... 1  
 Changed 10  $\mu F$  to 1  $\mu F$  in Output Capacitor Section ..... 12  
 Deleted Negative Precision Reference Without Precision Resistors Section ..... 14

**9/2011—Rev. 0 to Rev. A**

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**10/2006—Revision 0: Initial Version**

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## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $V_{IN} = 2.0\text{ V}$  to  $18\text{ V}$ , unless otherwise noted. SET (Pin 5) tied to  $V_{OUT}$  (Pin 4).

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE	$V_O$					
A Grade			0.49650	0.5	0.50350	V
B Grade			0.49825	0.5	0.50175	V
INITIAL ACCURACY ERROR	$V_{OERR}$					
A Grade			-3.50		+3.50	mV
B Grade			-1.75		+1.75	mV
TEMPERATURE COEFFICIENT	$TCV_O$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$				
A Grade				15	50	ppm/ $^\circ\text{C}$
B Grade				5	25	ppm/ $^\circ\text{C}$
LOAD REGULATION		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$ ; $3\text{ V} \leq V_{IN} \leq 18\text{ V}$ ; $0\text{ mA} < I_{OUT} < 4\text{ mA}$	-0.13		+0.13	mV/mA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$ ; $3\text{ V} \leq V_{IN} \leq 18\text{ V}$ ; $-2\text{ mA} < I_{OUT} < 0\text{ mA}$	-1.0		+1.0	mV/mA
LINE REGULATION		$2.0\text{ V}$ to $18\text{ V}$ , $I_{OUT} = 0\text{ mA}$	-40	+10	+40	ppm/V
QUIESCENT CURRENT	$I_Q$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$ , no load		75	150	$\mu\text{A}$
SHORT-CIRCUIT CURRENT TO GROUND		$V_{IN} = 2.0\text{ V}$		15		mA
		$V_{IN} = 18.0\text{ V}$		50		mA
VOLTAGE NOISE		0.1 Hz to 10 Hz		3		$\mu\text{V p-p}$
TURN-ON SETTLING TIME		To 0.1%, $C_{LOAD} = 0.1\ \mu\text{F}$		80		$\mu\text{s}$
LONG-TERM STABILITY		1000 hours at $25^\circ\text{C}$		100		ppm/1000 hours
OUTPUT VOLTAGE HYSTERESIS				150		ppm

$T_A = 25^\circ\text{C}$ ,  $V_{IN} = 2.0\text{ V}$  to  $18\text{ V}$ , unless otherwise noted. SET (Pin 5) tied to GND (Pin 2).

**Table 2.**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE	$V_O$		0.9930	1.0	1.0070	V
A Grade						
B Grade			0.9965	1.0	1.0035	V
INITIAL ACCURACY ERROR	$V_{OERR}$		-7.0		+7.0	mV
A Grade						
B Grade			-3.5		+3.5	mV
TEMPERATURE COEFFICIENT	$TCV_O$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		15	50	ppm/ $^\circ\text{C}$
A Grade						
B Grade			5	25	ppm/ $^\circ\text{C}$	
LOAD REGULATION		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$ ; $3\text{ V} \leq V_{IN} \leq 18\text{ V}$ ; $0\text{ mA} < I_{OUT} < 4\text{ mA}$	-0.25		+0.25	mV/mA
LINE REGULATION		$2.0\text{ V}$ to $18\text{ V}$ , $I_{OUT} = 0\text{ mA}$	-40	+10	+40	ppm/V
QUIESCENT CURRENT	$I_Q$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$ , no load		85	150	$\mu\text{A}$
SHORT-CIRCUIT CURRENT TO GROUND		$V_{IN} = 2.0\text{ V}$		15		mA
		$V_{IN} = 18.0\text{ V}$		50		mA
VOLTAGE NOISE		0.1 Hz to 10 Hz		6		$\mu\text{V p-p}$
TURN-ON SETTLING TIME		To 0.1%, $C_{LOAD} = 0.1\ \mu\text{F}$		80		$\mu\text{s}$
LONG-TERM STABILITY		1000 hours at $25^\circ\text{C}$		100		ppm/1000 hours
OUTPUT VOLTAGE HYSTERESIS				150		ppm

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Ratings
V <sub>IN</sub> to GND	20 V
Internal Power Dissipation	40 mW
Storage Temperature Range	−65°C to +150°C
Specified Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
6-Lead TSOT (UJ-6)	186	67	°C/W

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

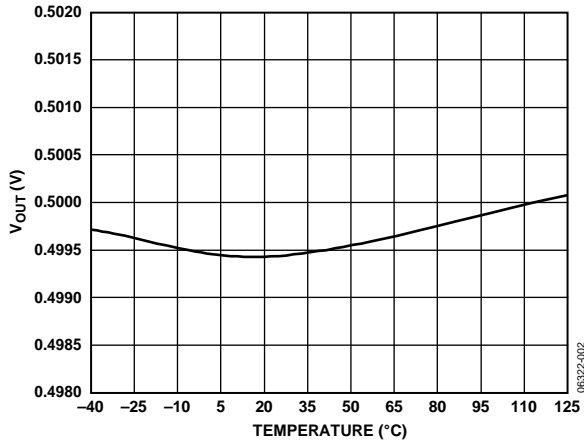


Figure 2.  $V_{OUT}$  vs. Temperature,  $V_{OUT} = 0.5 V$

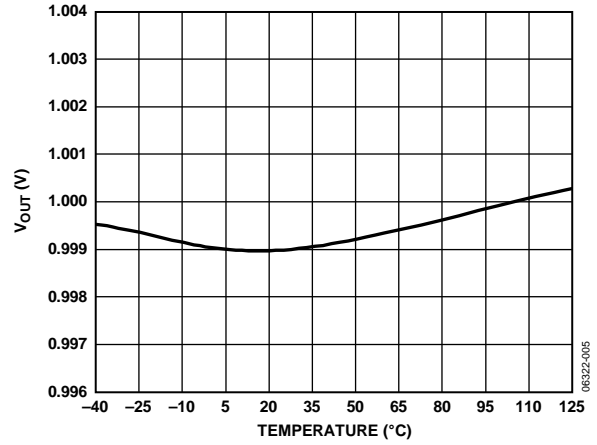


Figure 5.  $V_{OUT}$  vs. Temperature,  $V_{OUT} = 1 V$

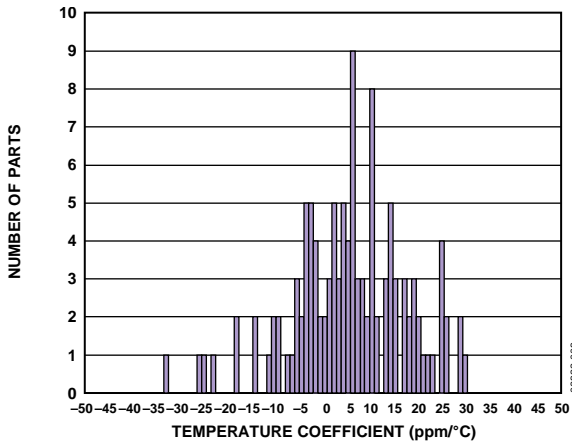


Figure 3. Temperature Coefficient,  $V_{OUT} = 0.5 V$

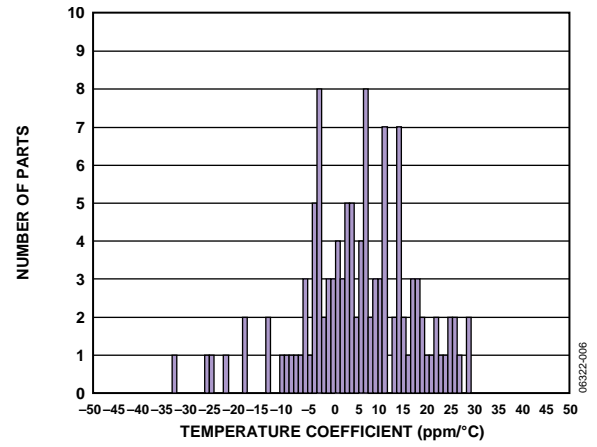


Figure 6. Temperature Coefficient,  $V_{OUT} = 1 V$

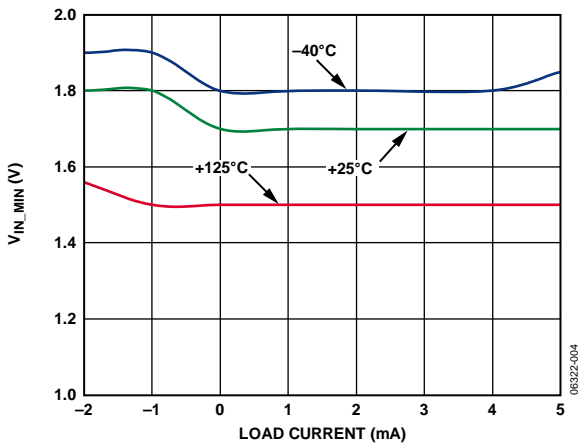


Figure 4. Minimum Input Voltage vs. Load Current,  $V_{OUT} = 0.5 V$

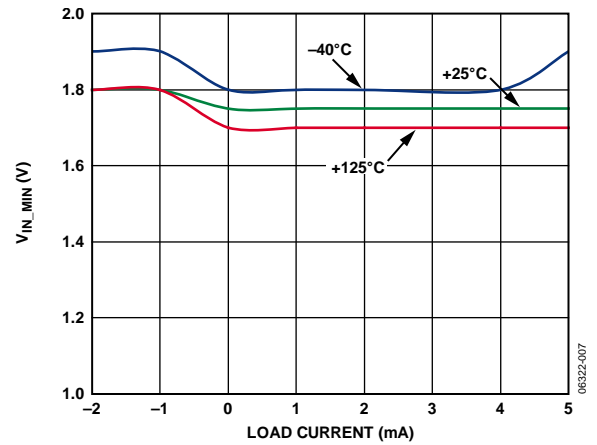


Figure 7. Minimum Input Voltage vs. Load Current,  $V_{OUT} = 1 V$

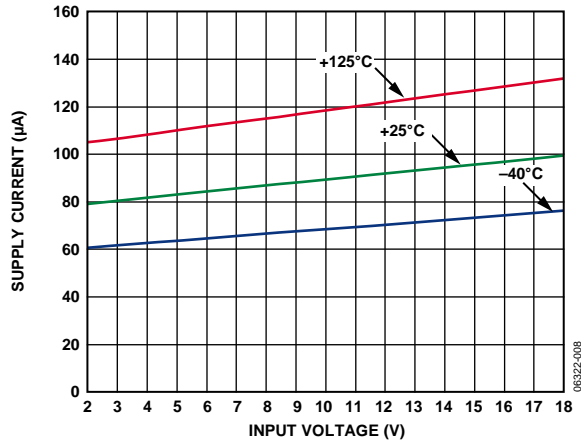


Figure 8. Supply Current vs. Input Voltage,  $V_{OUT} = 0.5 V$

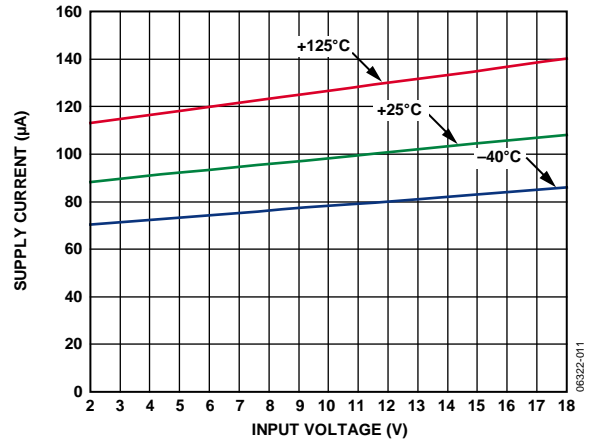


Figure 11. Supply Current vs. Input Voltage,  $V_{OUT} = 1 V$

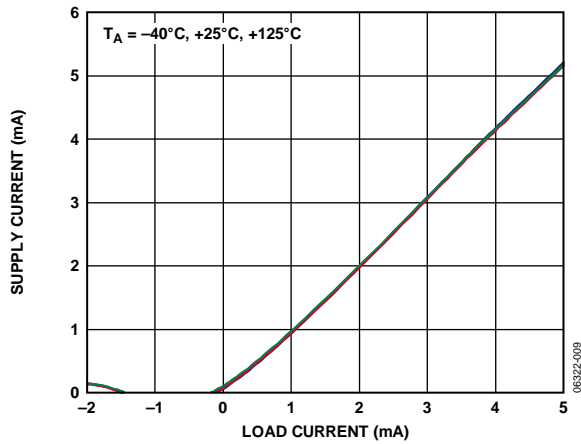


Figure 9. Supply Current vs. Load Current,  $V_{OUT} = 0.5 V$

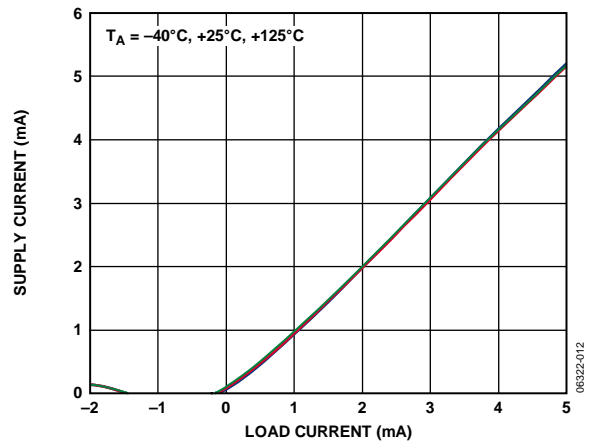


Figure 12. Supply Current vs. Load Current,  $V_{OUT} = 1 V$

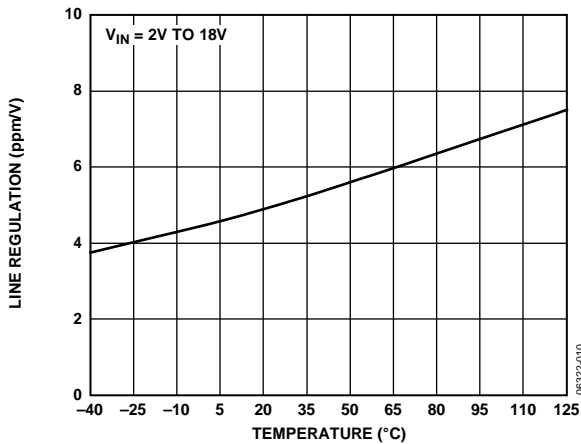


Figure 10. Line Regulation vs. Temperature,  $V_{OUT} = 0.5 V$

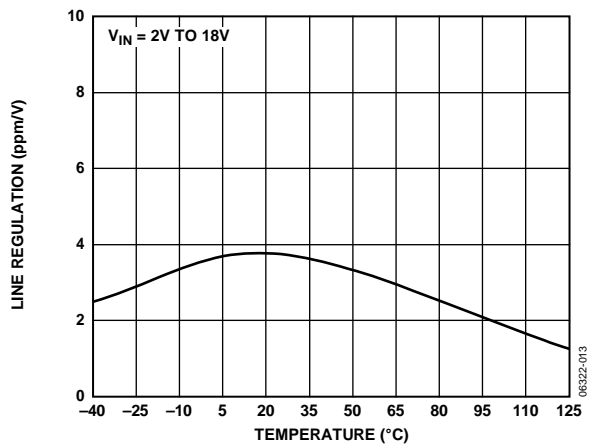


Figure 13. Line Regulation vs. Temperature,  $V_{OUT} = 1 V$

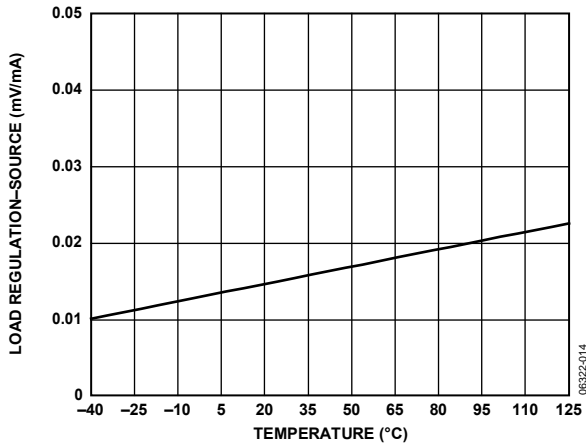


Figure 14. Load Regulation (Source) vs. Temperature,  $V_{OUT} = 0.5 V$

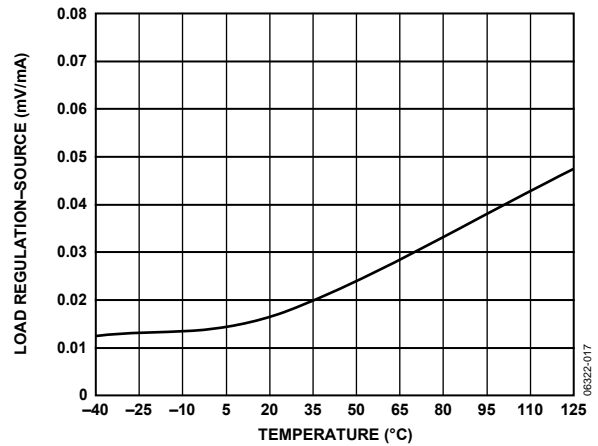


Figure 17. Load Regulation (Source) vs. Temperature,  $V_{OUT} = 1 V$

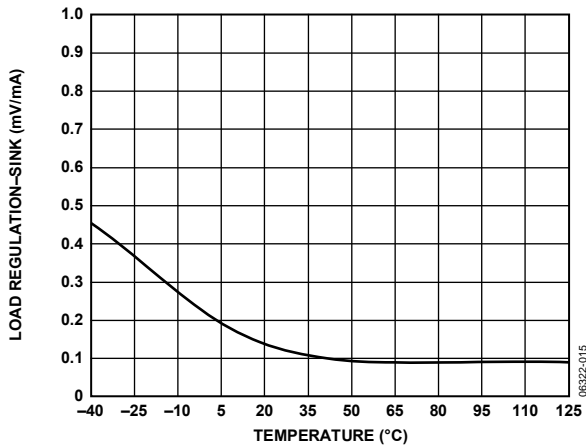


Figure 15. Load Regulation (Sink) vs. Temperature,  $V_{OUT} = 0.5 V$

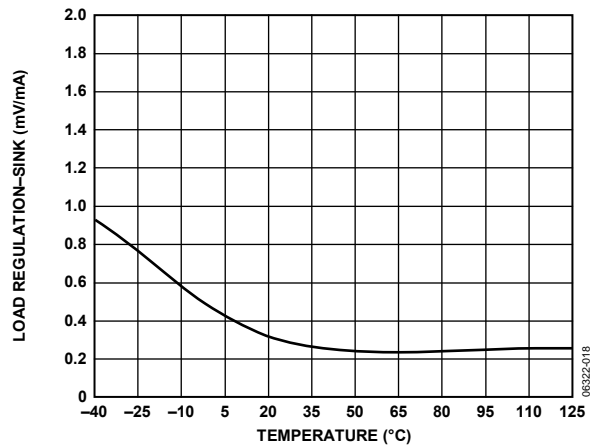


Figure 18. Load Regulation (Sink) vs. Temperature,  $V_{OUT} = 1 V$

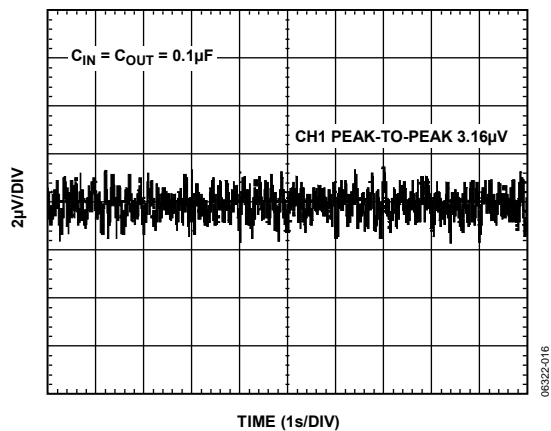


Figure 16. 0.1 Hz to 10 Hz Noise,  $V_{OUT} = 0.5 V$

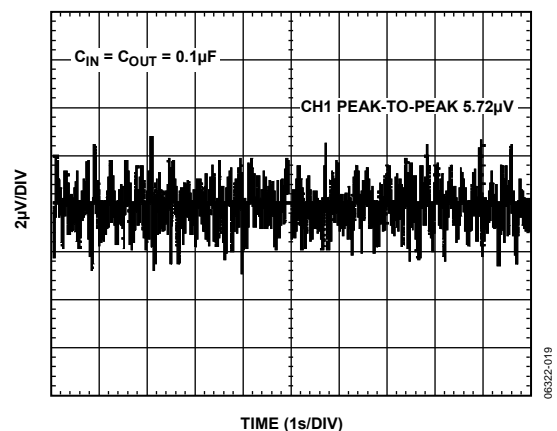


Figure 19. 0.1 Hz to 10 Hz Noise,  $V_{OUT} = 1 V$



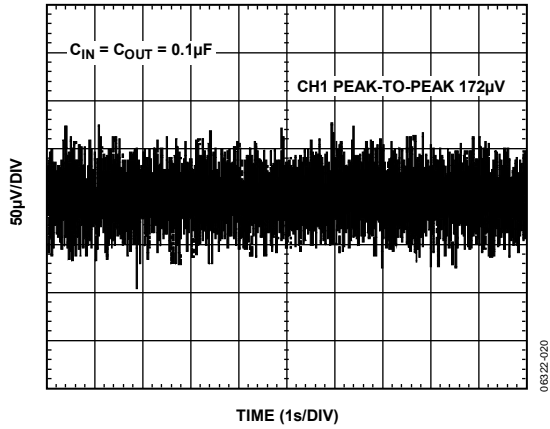


Figure 20. 10 Hz to 10 kHz Noise,  $V_{OUT} = 0.5 V$

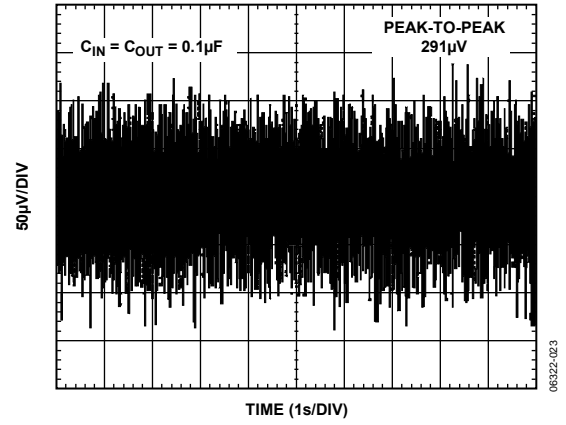


Figure 23. 10 Hz to 10 kHz Noise,  $V_{OUT} = 1 V$

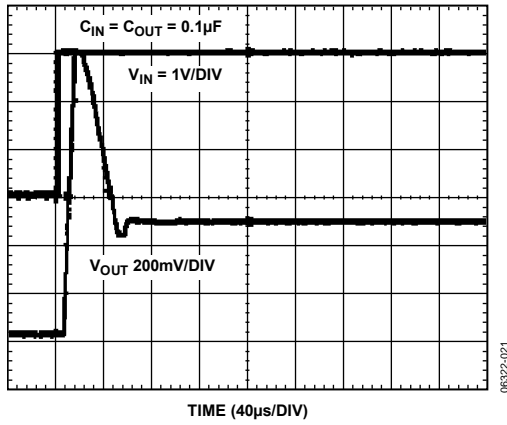


Figure 21. Turn-On Response,  $V_{OUT} = 0.5 V$

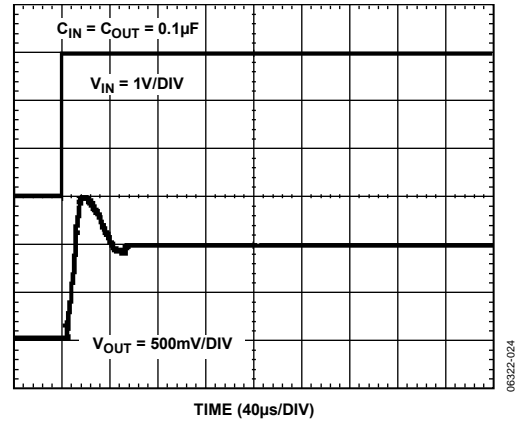


Figure 24. Turn-On Response,  $V_{OUT} = 1 V$

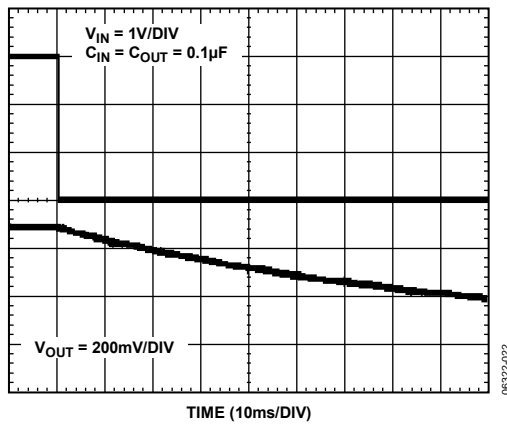


Figure 22. Turn-Off Response,  $V_{OUT} = 0.5 V$

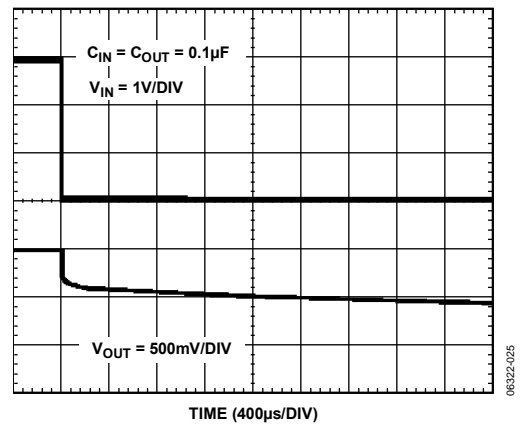


Figure 25. Turn-Off Response,  $V_{OUT} = 1 V$

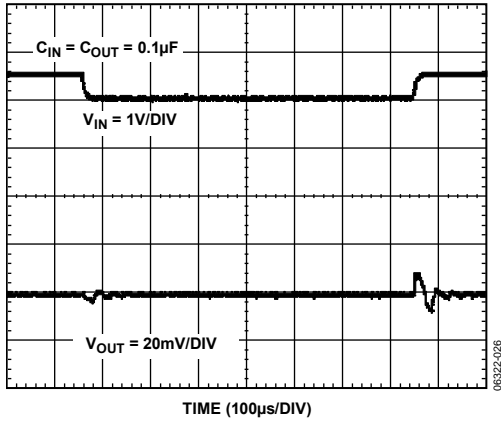


Figure 26. Line Transient Response,  $V_{OUT} = 0.5\text{ V}$

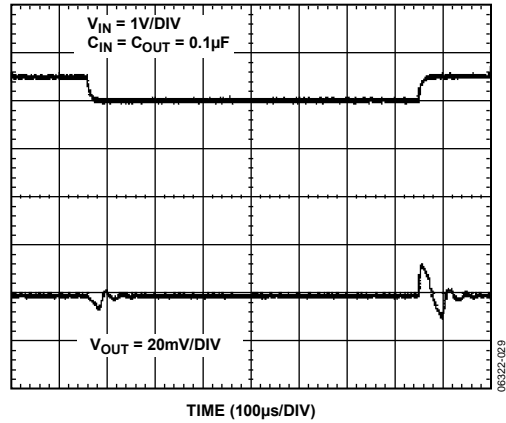


Figure 29. Line Transient Response,  $V_{OUT} = 1\text{ V}$

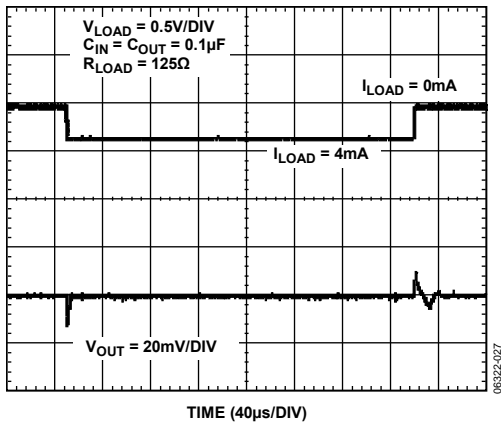


Figure 27. Load Transient Response (Source),  $V_{OUT} = 0.5\text{ V}$

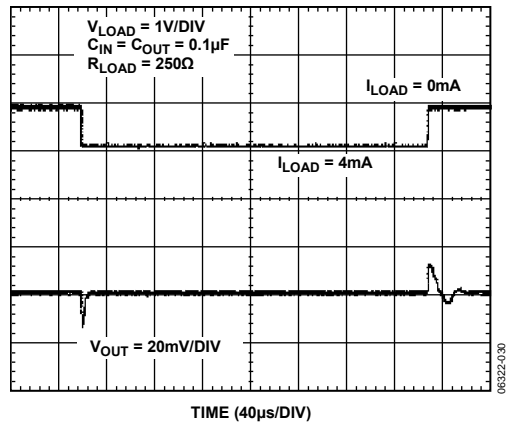


Figure 30. Load Transient Response (Source),  $V_{OUT} = 1\text{ V}$

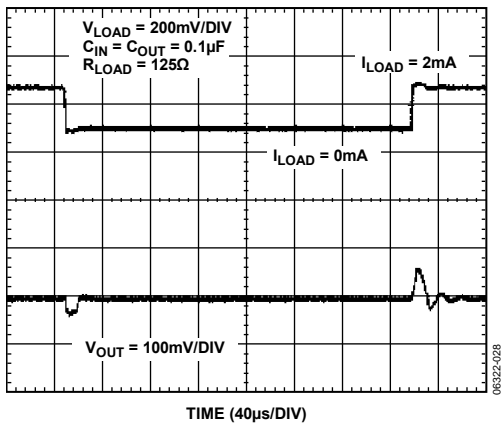


Figure 28. Load Transient Response (Sink),  $V_{OUT} = 0.5\text{ V}$

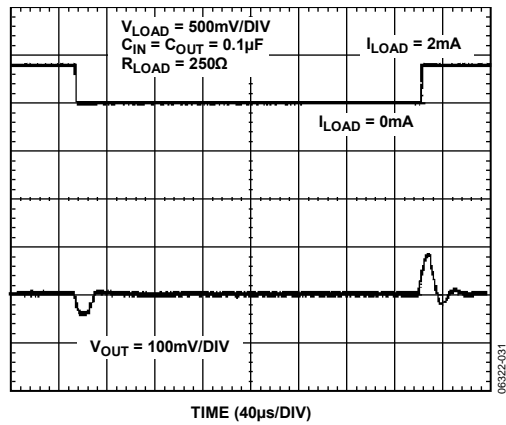


Figure 31. Load Transient Response (Sink),  $V_{OUT} = 1\text{ V}$

## TERMINOLOGY

### Temperature Coefficient

Temperature coefficient is the change of output voltage with respect to the operating temperature change normalized by the output voltage at 25°C. This parameter is expressed in ppm/°C and is determined by

$$TCV_O [\text{ppm}/^\circ\text{C}] = \frac{V_O(T_2) - V_O(T_1)}{V_O(25^\circ\text{C}) \times (T_2 - T_1)} \times 10^6$$

where:

$V_O(25^\circ\text{C}) = V_O$  at 25°C.

$V_O(T_1) = V_O$  at Temperature 1.

$V_O(T_2) = V_O$  at Temperature 2.

### Line Regulation

Line regulation is the change in the output due to a specified change in input voltage. This parameter accounts for the effects of self-heating. Line regulation is expressed in either %/V, ppm/V, or  $\mu\text{V}/\Delta V_{\text{IN}}$ .

### Load Regulation

Load regulation is the change in output voltage due to a specified change in load current. This parameter accounts for the effects of self-heating. Load regulation is expressed in either mV/mA, ppm/mA, or dc output resistance ( $\Omega$ ).

### Long-Term Stability

Long-term stability is the typical shift of output voltage at 25°C on a sample of parts subjected to a test of 1000 hours at 25°C.

$$\Delta V_O = V_O(t_0) - V_O(t_1)$$

$$\Delta V_O [\text{ppm}] = \frac{V_O(t_0) - V_O(t_1)}{V_O(t_0)} \times 10^6$$

where:

$V_O(t_0) = V_O$  at 25°C at Time 0.

$V_O(t_1) = V_O$  at 25°C after 1000 hours operating at 25°C.

### Thermal Hysteresis

Thermal hysteresis is the change of output voltage after the device is cycled through temperatures from +25°C to -40°C to +125°C, then back to +25°C. This is a typical value from a sample of parts put through such a cycle.

where:

$V_O(25^\circ\text{C}) = V_O$  at 25°C.

$V_{\text{OTC}} = V_O$  at 25°C after temperature cycle from +25°C to -40°C to +125°C, then back to +25°C.

## THEORY OF OPERATION

The [ADR130](#) sub-band gap reference is the high performance solution for low supply voltage and low power applications. The uniqueness of this product lies in its architecture.

### POWER DISSIPATION CONSIDERATIONS

The [ADR130](#) is capable of delivering load currents to 4 mA with an input range from 3.0 V to 18 V. When this device is used in applications with large input voltages, care must be taken to avoid exceeding the specified maximum power dissipation or junction temperature, because this results in premature device failure.

Use the following formula to calculate the maximum junction temperature or dissipation:

$$P_D = \frac{T_J - T_A}{\theta_{JA}}$$

where:

$T_J$  is the junction temperature.

$T_A$  is the ambient temperature.

$P_D$  is the device power dissipation.

$\theta_{JA}$  is the device package thermal resistance.

### INPUT CAPACITOR

Input capacitors are not required on the [ADR130](#). There is no limit for the value of the capacitor used on the input, but a 1  $\mu\text{F}$  to 10  $\mu\text{F}$  capacitor on the input improves transient response in applications where there is a sudden supply change. An additional 0.1  $\mu\text{F}$  capacitor in parallel also helps reduce noise from the supply.

### OUTPUT CAPACITOR

The [ADR130](#) requires a small 0.1  $\mu\text{F}$  output capacitor for stability. Additional 0.1  $\mu\text{F}$  to 1  $\mu\text{F}$  capacitance in parallel can improve load transient response. This acts as a source of stored energy for a sudden increase in load current. The only parameter that is affected by the additional capacitance is turn-on time.

## APPLICATION NOTES

### BASIC VOLTAGE REFERENCE CONNECTION

The circuits in Figure 32 and Figure 33 illustrate the basic configuration for the ADR130 voltage reference.

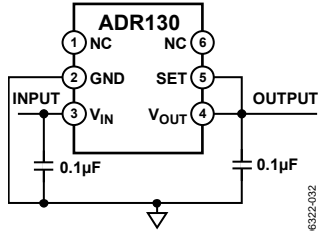


Figure 32. Basic Configuration,  $V_{OUT} = 0.5\text{ V}$

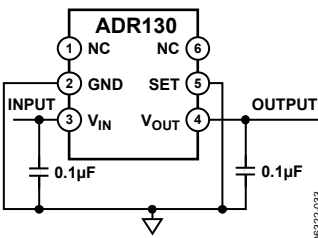


Figure 33. Basic Configuration,  $V_{OUT} = 1\text{ V}$

### STACKING REFERENCE ICs FOR ARBITRARY OUTPUTS

Some applications may require two reference voltage sources that are a combined sum of the standard outputs. Figure 34 and Figure 35 show how these stacked output references can be implemented.

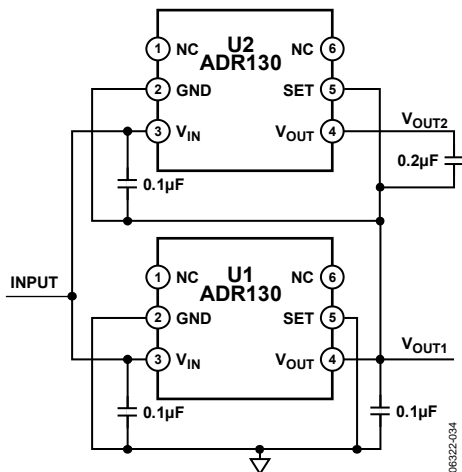


Figure 34. Stacking References with ADR130,  $V_{OUT1} = 1.0\text{ V}$ ,  $V_{OUT2} = 2.0\text{ V}$

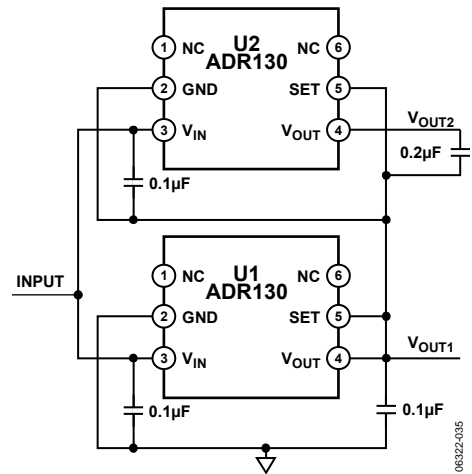


Figure 35. Stacking References with ADR130,  $V_{OUT1} = 0.5\text{ V}$ ,  $V_{OUT2} = 1.5\text{ V}$

Two reference ICs are used and fed from an unregulated input,  $V_{IN}$ . The outputs of the individual ICs that are connected in series provide two output voltages,  $V_{OUT1}$  and  $V_{OUT2}$ .  $V_{OUT1}$  is the terminal voltage of U1, and  $V_{OUT2}$  is the sum of this voltage and the terminal voltage of U2. U1 and U2 are chosen for the two voltages that supply the required outputs (see Table 5). For example, if U1 is set to have an output of 1 V or 0.5 V, the user can stack on top of U2 to get an output of 2 V or 1.5 V.

Table 5. Required Outputs

U1/U2	Comments	$V_{OUT1}$	$V_{OUT2}$
ADR130/ADR130	See Figure 34	1 V	2 V
ADR130/ADR130	See Figure 35	0.5 V	1.5 V

**PRECISION CURRENT SOURCE**

In low power applications, the need can arise for a precision current source that can operate on low supply voltages. The [ADR130](#) can be configured as a precision current source (see Figure 36). The circuit configuration shown is a floating current source with a grounded load. The reference output voltage is bootstrapped across  $R_{SET}$ , which sets the output current into the load. With this configuration, circuit precision is maintained for load currents ranging from the reference supply current, typically  $85\ \mu\text{A}$ , to approximately  $4\ \text{mA}$ .

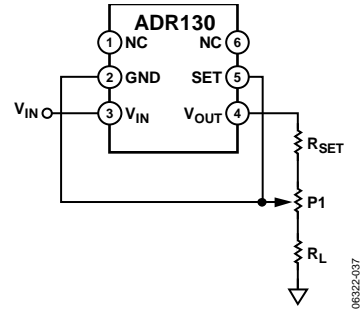
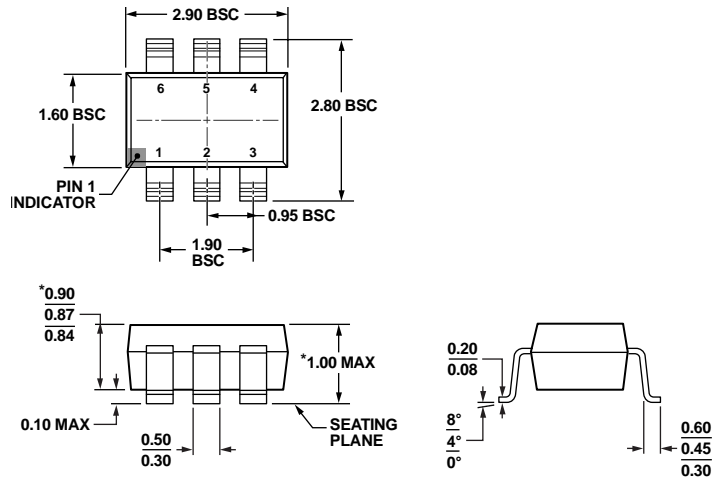


Figure 36. [ADR130](#) as a Precision Current Source

# OUTLINE DIMENSIONS



\*COMPLIANT TO JEDEC STANDARDS MO-193-AA WITH THE EXCEPTION OF PACKAGE HEIGHT AND THICKNESS.

Figure 37. 6-Lead Thin Small Outline Transistor Package [TSOT] (UJ-6)  
Dimensions shown in millimeters

102806-A

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Coefficient (ppm/°C)	Temperature Range	Package Description	Package Option	Marking Code	Ordering Quantity
ADR130AUJZ-REEL7	50	-40°C to +125°C	6-Lead TSOT	UJ-6	R0W	3,000
ADR130BUJZ-REEL7	25	-40°C to +125°C	6-Lead TSOT	UJ-6	R0X	3,000

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**