PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPG-PWR/14/8422
Dated 11 Apr 2014

D2PAK ECOPACK 2 graded moulding compound assembly capacity expansion - Subcontractor Ase Weihai (China)

Table 1. Change Implementation Schedule

Forecasted implementation date for change	04-Apr-2014
Forecasted availability date of samples for customer	04-Apr-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	04-Apr-2014
Estimated date of changed product first shipment	11-Jul-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Package assembly material change
Reason for change	To improve service to Customers by increasing productivity as ECOPACK 2
Description of the change	Following the continuous improvement of our service and in order to rationalize and optimize Power MOSFET Transistors productivity, this document is announcing that D2PAK products, listed in this PCN, will be also produced in Subcontractor Ase Weihai (China), according to the program to introduce ECOPACK 2 grade products. Ase Weihai D2PAK package, guarantee the same quality and electrical characteristics as reported in the relevant data sheets. Devices used for qualification are available as samples
Change Product Identification	Will be identified with a letter "G" printed in the ECO Level field
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

✂

Customer Acknowledgement of Receipt **PCN IPG-PWR/14/8422**

Please sign and return to STMicroelectronics Sales Office **Dated 11 Apr 2014**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

DOCUMENT APPROVAL

Name	Function
Mottese, Anna	Marketing Manager
Aleo, Mario-Antonio	Product Manager
Falcone, Giuseppe	Q.A. Manager

Dear Customer,

Please be informed that D^2PAK of Power MOSFET Transistors, manufactured in Subcontractor Ase Weihai (China), will be also produced, according to the program to introduce ECOPACK 2 grade products.

The involved product series and affected packages are listed in the table below:

Product Family	Package	Commercial Product / Series
Power MOSFET Transistors	D^2PAK	See Product list

Any other product related to the above series, manufactured in D^2PAK package, even if not expressly included or partially mentioned in the attached table, is affected by this change.

<u>Qualification program and results availability</u>:

The reliability test report is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 13-2014.
Any other sample request will be processed and scheduled by Power Transistor Division upon request.

Product Family	Part Number - Test Vehicle
Power MOSFET Transistors	STB80NF10T4 STB9NK50ZT4

<u>Change implementation schedule:</u>

The production start and first shipments will be implemented according to our work in progress and materials availability:

Product Family	1st Shipments
Power MOSFET Transistors	From Week 26-2014

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 days period will constitute acceptance of the change (Jedec Standard No. 46-C). In any case, first shipments may start earlier with customer written agreement.

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of D^2PAK green resin, manufactured in Ase Weihai (China), will be identified with a letter “G” printed in the ECO Level field.

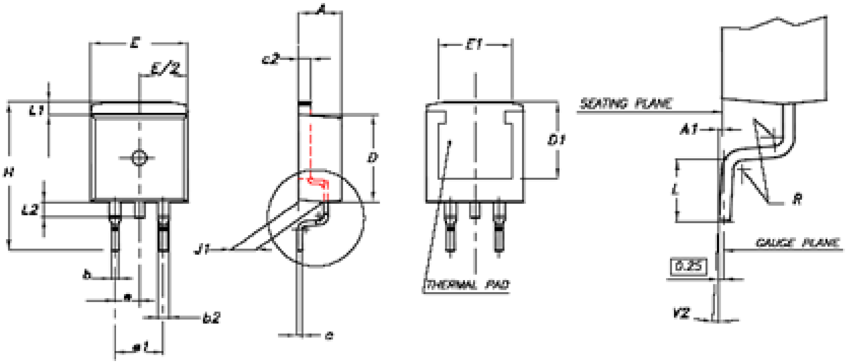
Sincerely Yours

ASE Weihai D^{2}PAK Package Comparison

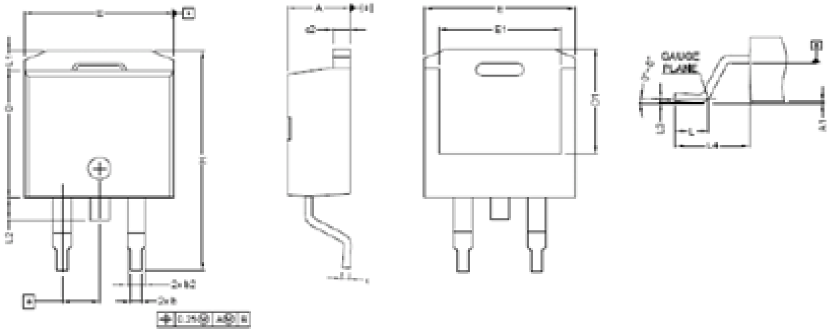
Symbol	ASE WEIHAI OLD POA (mm)			ASE WEIHAI NEW POA (mm)			ST POA (mm)		
	Nom	Min	Max	Nom	Min	Max	Nom	Min	Max
A		4.30	4.70		4.36	4.6		4.40	4.60
A1		0	0.20		0	0.25		0.03	0.023
b		0.70	0.90		0.70	0.93		0.70	0.93
b2		1.17	1.37		1.14	1.7		1.14	1.70
c	0.5	0.45	0.60		0.38	0.694		0.45	0.60
c2	1.3	1.25	1.40		1.19	1.36		1.23	1.36
D	9.2	9	9.40		8.6	9.35		8.95	9.35
D1		7.50			6.9			7.5	
E		9.80	10.20		10	10.55		10	10.4
E1		7.50			8.1			8.5	
e	2.54			2.54			2.54		
e1	5.08				-			4.88	5.28
H	15.3	15	15.60		15.0	15.85		15	15.85
J1		2.20	2.60		-	-		2.49	2.69
L		1.79	2.79		1.9	2.79		2.29	2.79
L1		1	1.40		-	1.65		1.27	1.40
L2		1.2	1.6			1.78		1.3	1.75
R	0.3				-		0.4		
V2		0º	3º		0º	8º		0º	8º

ASE Weihai D^2PAK Package

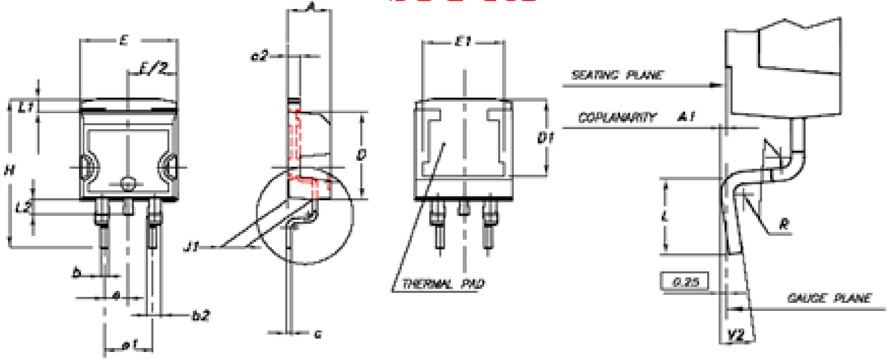
ASE WEIHAI OLD POA



ASE WEIHAI NEW POA

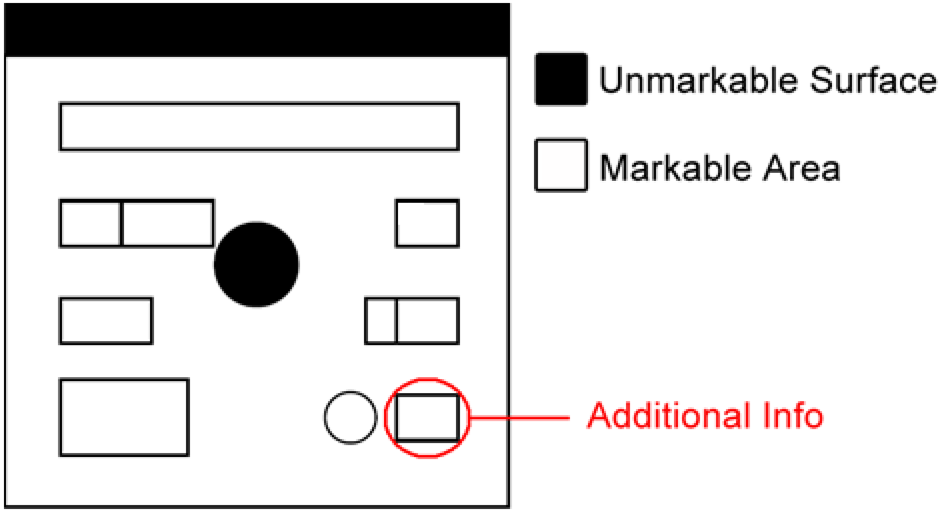


ST POA

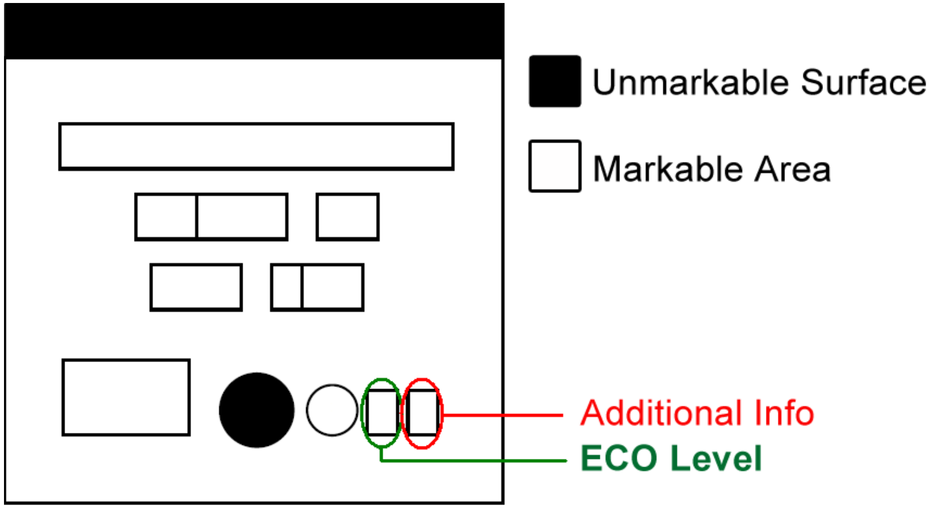


ASE Weihai D^{2}PAK Package Comparison

Current Marking Composition



New Marking Composition



ECOPACK®2 Marking Traceability

Reliability Report

D^{2}PAK ECOPACK®2 graded molding compound assembly capacity expansion – Subcontractor Ase Weihai (China)

General Information	
Product Lines:	MM0J – EZ54
Product Families:	Power MOSFET
P/Ns:	STB80NF10T4 (MM0J) STB9NK50ZT4 (EZ54)
Product Group:	IMS - IPG
Product division:	Power Transistor Division
Package:	D^{2}PAK
Silicon Process techn.:	low gate charge STripFET™ II Zener-Protected SuperMESH™

Locations	
Wafer Diffusion Plants:	*Ang Mo Kio (Singapore)*
EWS Plants:	*Ang Mo Kio (Singapore)*
Assembly plant:	*Ase Weihai (China)*
Reliability Lab:	*IMS-IPG Catania Reliability Lab.*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	October 2013	8	C. Cappello	G. Falcone	First issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualification of the D^2PAK package graded Molding Compound manufactured in Subcontractor Ase Weihai (China).

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

N-channel Power MOSFET

4.2 Construction note

D.U.T.: STB80NF10T4 LINE: MM0J PACKAGE: D^2PAK

Wafer/Die fab. information	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	StripFET™II
Die finishing back side	Ti/Ni/Au
Die size	4610 x 5660 μm^2
Metal	Al/Si/Cu
Passivation type	None

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	Ase Weihai (China)
Package description	D^2PAK
Molding compound	HF Epoxy Resin
Frame material	Bare Copper
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Ultrasonic
Wires bonding materials	Al 5 mils Gate Al 15 mils Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Ase Weihai (China)
Tester	STATEC

D.U.T.: STB9NK50ZT4 LINE: EZ54 PACKAGE: D^{2}PAK

Wafer/Die fab. information	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	SuperMESH™
Die finishing back side	Ti/Ni/Au
Die size	4086 x 3434 µm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Ang Mo Kio (Singapore)*
Test program	WPIS

Assembly information	
Assembly site	Ase Weihai (China)
Package description	D^{2}PAK
Molding compound	HF Epoxy Resin
Frame material	Bare Copper
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Ultrasonic
Wires bonding materials	Al 5 mils Gate Al 10 mils Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Ase Weihai (China)
Tester	STATEC

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	STB80NF10T4	MM0J	Power MOSFET
2	STB9NK50ZT4	EZ54	Power MOSFET

5.2 Reliability test plan summary

Lot. 1 - D.U.T.: STB80NF10T4 LINE: MM0J PACKAGE: D^{2}PAK

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
						Lot 1
Die Oriented Tests						
HTRB	N	JESD22 A-108	T.A.=175°C Vdss=80V	77	168 H 500 H 1000 H	0/77
HTGB	N	JESD22 A-108	TA = 150°C Vgss= 20V	77	168 H 500 H 1000 H	0/77
HTSL	N	JESD22 A-103	TA = 175°C	77	168 H 500 H 1000 H	0/77
Package Oriented Tests						
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=245°C for 3 times	251	Final	0/251
H3TRB	Y	JESD22 A-101	Ta=85°C Rh=85%, Vdss=80V	77	168 H 500 H 1000 H	0/77
TC	Y	JESD22 A-104	TA=-65°C TO 150°C (1 HOUR/CYCLE)	77	100 cy 200 cy 500 cy 1000 cy	0/77
TF/IOL	Y	Mil-STD 750D Method 1037	ΔTc=+105°C	20	5K cy 10K cy	0/20
AC	Y	JESD22 A-102	TA=121°C – PA=2 ATM	77	96 H	0/77

Lot. 2 - D.U.T.: STB9NK50ZT4 LINE: EZ54 PACKAGE: D^{2}PAK

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
						Lot 2
Die Oriented Tests						
HTRB	N	JESD22 A-108	T.A.=150°C Vdss=400V	77	168 H 500 H 1000 H	0/77
HTGB	N	JESD22 A-108	TA = 150°C Vgss= 30V	77	168 H 500 H 1000 H	0/77
HTSL	N	JESD22 A-103	TA = 150°C	77	168 H 500 H 1000 H	0/77
Package Oriented Tests						
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=245°C for 3 times	251	Final	0/251
H3TRB	Y	JESD22 A-101	Ta=85°C Rh=85%, Vdss=100V	77	168 H 500 H 1000 H	0/77
TC	Y	JESD22 A-104	TA=-65°C TO 150°C (1 HOUR/CYCLE)	77	100 cy 200 cy 500 cy 1000 cy	0/77
TF/IOL	Y	Mil-STD 750D Method 1037	∆Tc=+105°C	20	5K cy 10K cy	0/20
AC	Y	JESD22 A-102	TA=121°C – PA=2 ATM	77	96 H	0/77

6 ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
Die Oriented Tests		
HTRB High Temperature Reverse Bias **HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented Tests		
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	To verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.

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