



Features

- ESD Protect for 1 Line with Bi-directional
- Provide ESD protection for the protected line to IEC 61000-4-2 (ESD) $\pm 20\text{kV}$ (air / contact)
IEC 61000-4-4 (EFT) 50A (5/50ns)
IEC 61000-4-5 (Lightning) 5A (8/20 μs)
- **0201 small DFN package** saves board space
- Protect one I/O line or one power line
- Fast turn-on and Low clamping voltage
- For low operating voltage applications: 3.3V maximum
- Solid-state silicon-avalanche and active circuit triggering technology
- Green Part

Applications

- Mobile Phones
- Hand Held Portable Applications
- Computer Interfaces Protection
- Microprocessors Protection
- Serial and Parallel Ports Protection
- Control Signal Lines Protection
- Power lines on PCB Protection
- Latchup Protection

Description

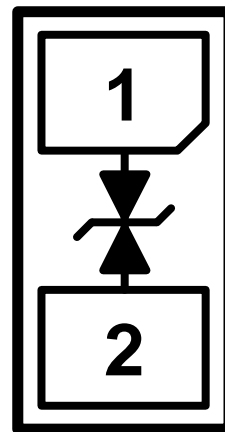
AZ5A23-01F is a design which includes one Bi-directional ESD rated clamping cell to protect one power line, or one control line, or one low speed data line in an electronic systems. The AZ5A23-01F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Cable Discharge Event (CDE).

AZ5A23-01F is a unique design which includes

proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ5A23-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge)

Circuit Diagram / Pin Configuration



DFN0603P2Y (Bottom View)
(0.6mm x 0.3mm x 0.3mm)



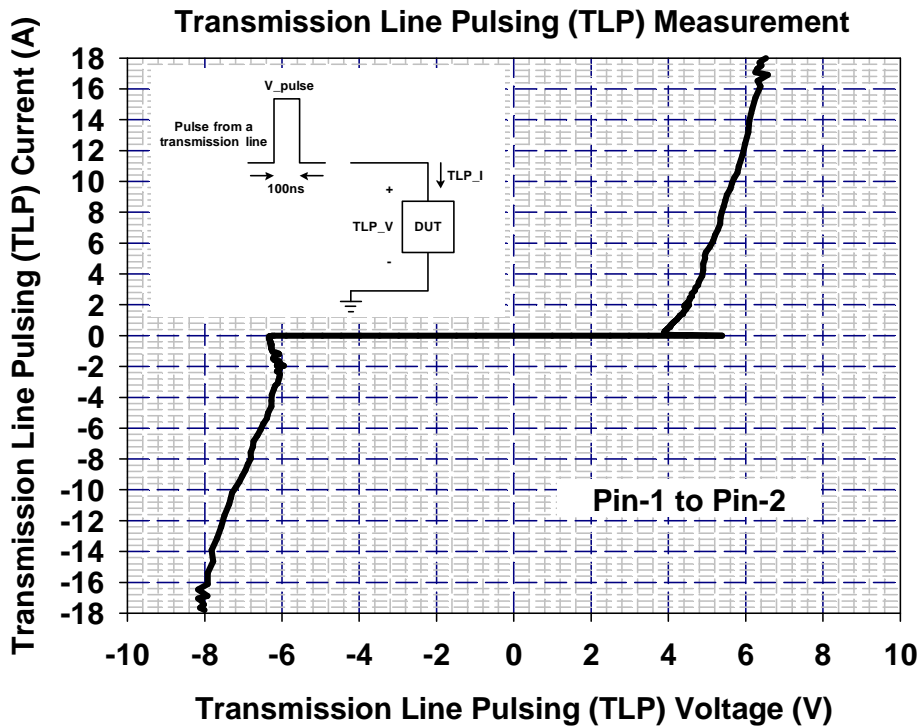
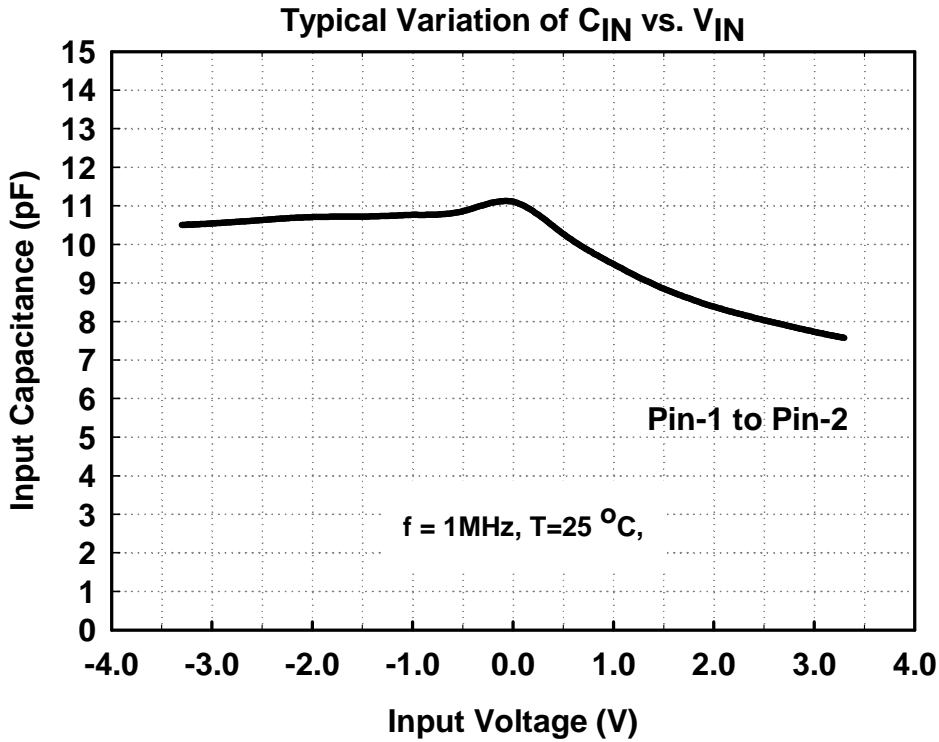
SPECIFICATIONS

| ABSOLUTE MAXIMUM RATINGS | | | |
|---------------------------------|------------------|---------------|-------|
| PARAMETER | SYMBOL | RATING | UNITS |
| Peak Pulse Current (tp =8/20μs) | I _{PP} | 5 | A |
| Operating Supply Voltage | V _{DC} | ±3.6 | V |
| ESD per IEC 61000-4-2 (Air) | V _{ESD} | ±20 | kV |
| ESD per IEC 61000-4-2 (Contact) | | ±20 | |
| Lead Soldering Temperature | T _{SOL} | 260 (10 sec.) | °C |
| Operating Temperature | T _{OP} | -55 to +85 | °C |
| Storage Temperature | T _{STO} | -55 to +150 | °C |

| ELECTRICAL CHARACTERISTICS | | | | | | |
|----------------------------|---------------------|--|------|-----|-----|-------|
| PARAMETER | SYMBOL | CONDITIONS | MINI | TYP | MAX | UNITS |
| Stand-Off Voltage | V _{RVM} | T=25 °C. | -3.3 | | 3.3 | V |
| Leakage Current | I _{Leak} | V _{RVM} = ±3.3V, T=25 °C. | | | 0.5 | μA |
| Breakdown Voltage | V _{BV} | I _{BV} = 1mA, T=25 °C. | 3.8 | | 6.8 | V |
| ESD Clamping Voltage | V _{ESD_CL} | IEC 61000-4-2 +6kV, T=25 °C, Contact mode. | | 8 | | V |
| Channel Input Capacitance | C _{IN} | V _R = 0V, f = 1MHz, T=25 °C. | | 11 | 15 | pF |



Typical Characteristics





Applications Information

The AZ5A23-01F is designed to protect one line against System ESD/EFT/Cable-Discharge pulses by clamping it to an acceptable reference. It provides bi-directional protection.

The usage of the AZ5A23-01F is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin 1. The pin 2 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ5A23-01F should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ5A23-01F.
- Place the AZ5A23-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

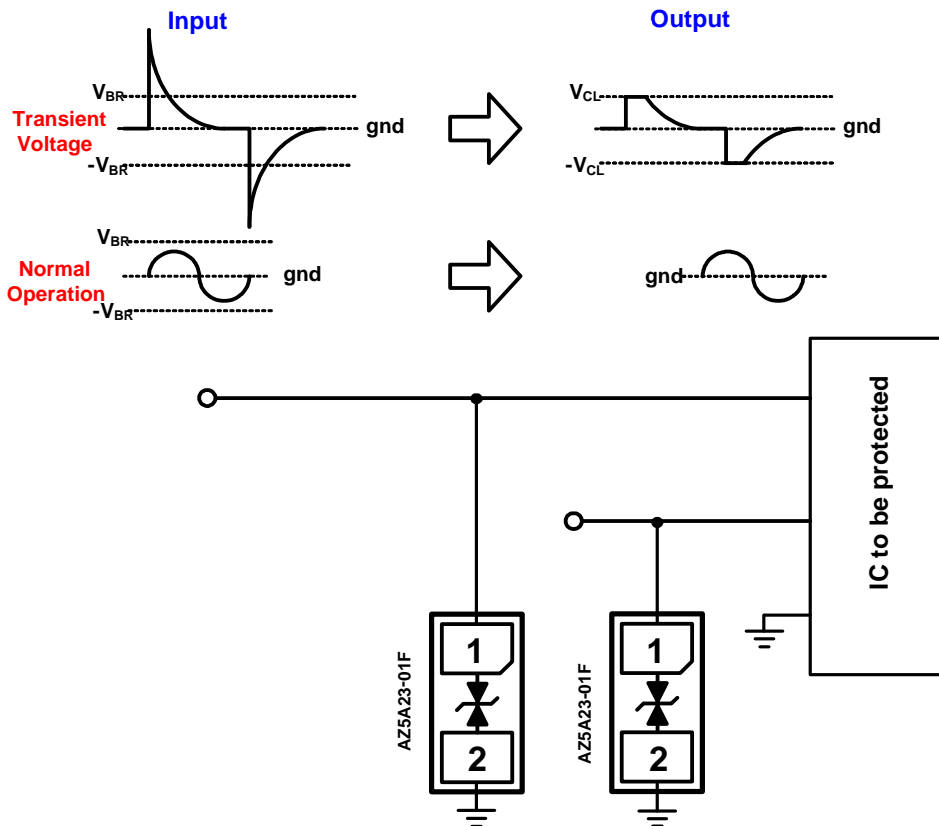


Fig. 1



Fig. 2 shows another simplified example of using AZ5A23-01F to protect the control line, low speed data line, and power line from ESD transient stress.

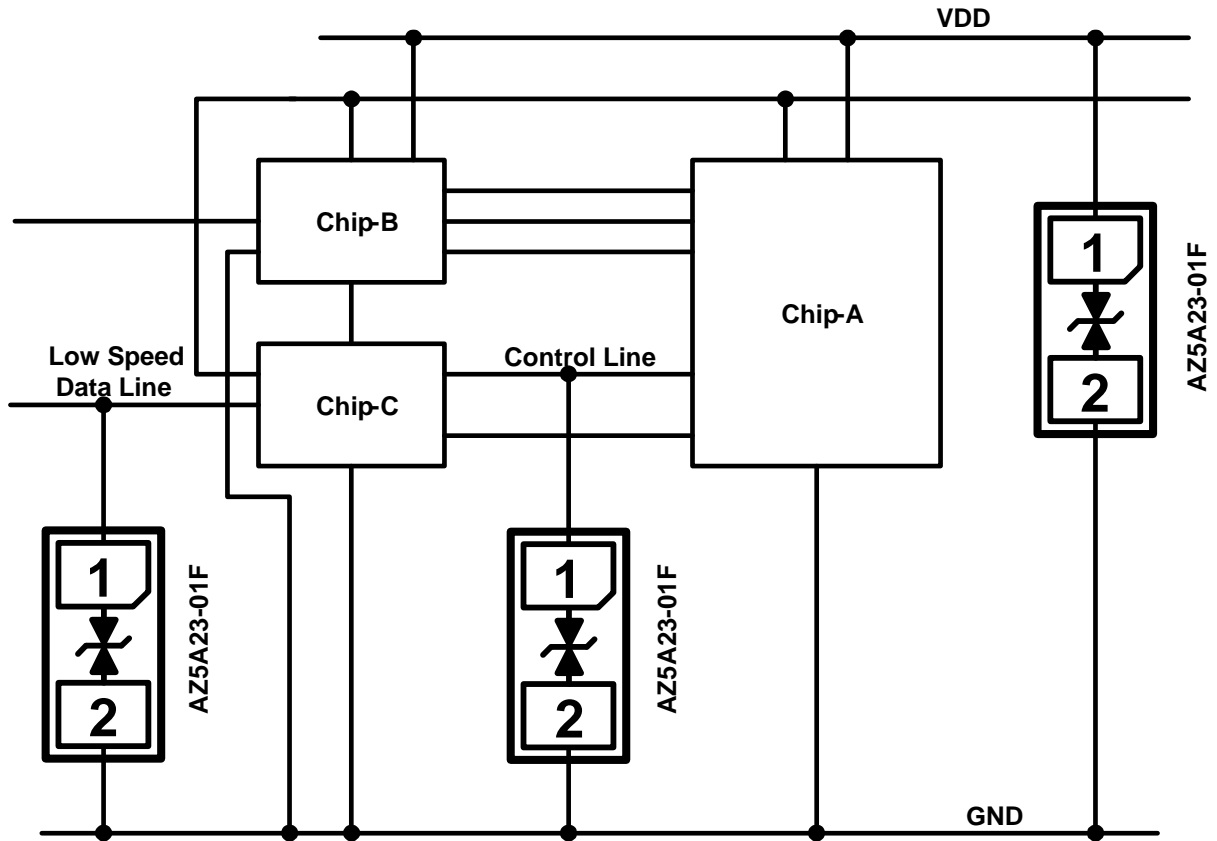
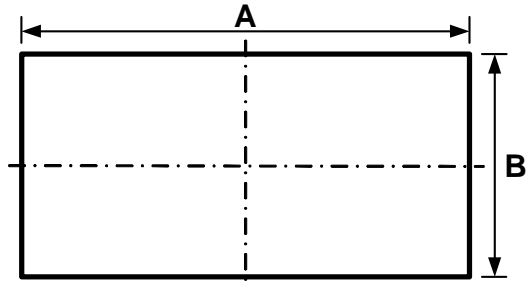


Fig. 2

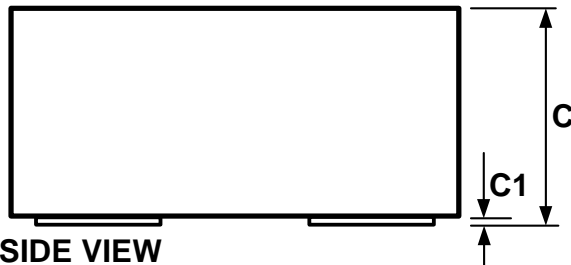


Mechanical Details

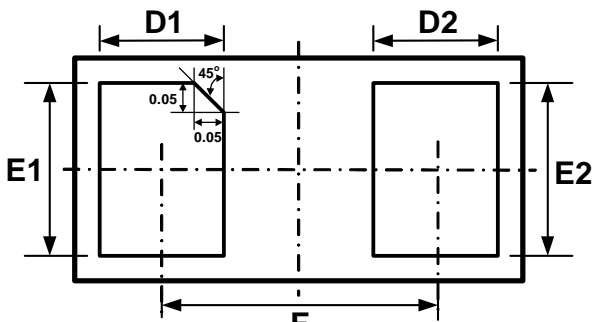
DFN0603P2Y PACKAGE DIAGRAMS



TOP VIEW



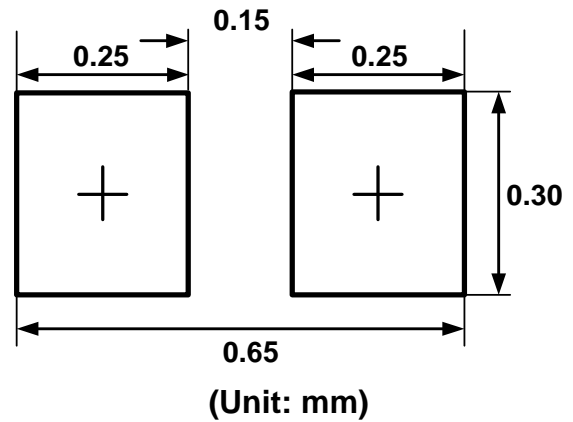
SIDE VIEW



BOTTOM VIEW

| SYMBOL | Millimeters | | |
|--------|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.55 | 0.60 | 0.65 |
| B | 0.25 | 0.30 | 0.35 |
| C | 0.28 | 0.30 | 0.32 |
| C1 | 0.00 | 0.02 | 0.05 |
| D1 | 0.13 | 0.18 | 0.23 |
| D2 | 0.14 | 0.19 | 0.24 |
| E1/E2 | 0.20 | 0.25 | 0.30 |
| F | 0.35 | | |

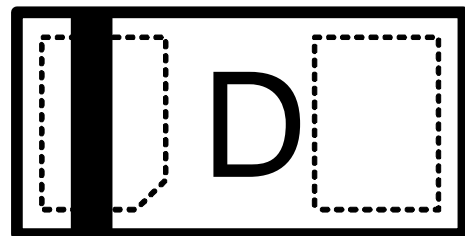
LAND LAYOUT



Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



| Part Number | Marking Code |
|-------------|--------------|
| AZ5A23-01F | D |

Note. Green means Pb-free, RoHS, and Halogen free compliant.



Ordering Information

| PN# | Material | Type | Reel size | MOQ | MOQ/internal box | MOQ/carton |
|----------------|----------|------|-----------|-------------|--------------------|-----------------------|
| AZ5A23-01F.R7G | Green | T/R | 7 inch | 12,000/reel | 4 reel= 48,000/box | 6 box =288,000/carton |

Revision History

| Revision | Modification Description |
|---------------------|---|
| Revision 2013/11/28 | Preliminary Release. |
| Revision 2014/05/16 | Update the max. spec of capacitance. |
| Revision 2014/09/05 | 1. Update the level of ESD and Lightning. 2. Formal Release. |
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