N+1 and ORing Power Rail Controller with Enable

Check for Samples: TPS2419

FEATURES

- **Control External FET for N+1 and ORing**
- **Controls Buses From 3 V to 16.5 V**
- **External Enable**
- **N-Channel MOSFETControl**
- **Rapid Device Turnoff Protects Bus Integrity**
- **Programmable Turn-Off Threshold**
- **Soft Turn on Reduces Bus Transients**
- **Industrial Temperature Range: –40°C to 85°C**
- **8-Pin TSSOP and SOIC Packages**

APPLICATIONS

- **N+1 Power Supplies**
- **Server Blades**
- **Telecom Systems**
- **High Availability Power Modules**

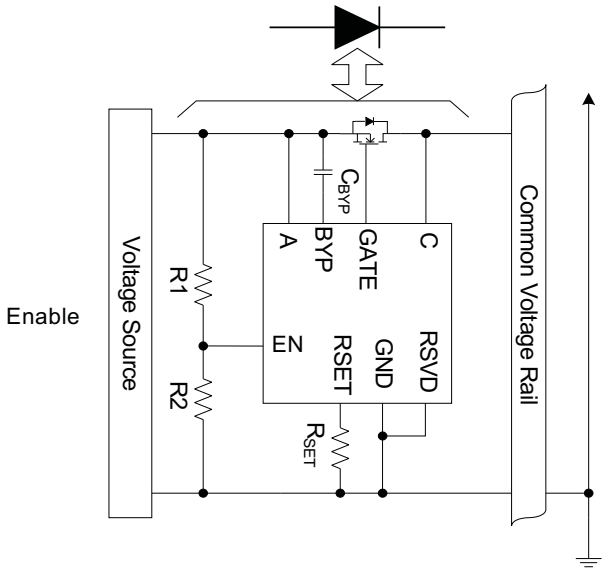


Figure 1. Typical Application

DESCRIPTION

The TPS2419 controller, in conjunction with an external N-channel MOSFET, provides the reverse current protection of an ORing diode with the efficiency of a MOSFET. The TPS2419 can be used to combine multiple power supplies to a common bus in an N+1 configuration, or to combine redundant input power buses.

Applications for the TPS2419 include a wide range of systems including servers and telecom. These applications often have either N+1 redundant power supplies, redundant power buses, or both. Redundant power sources must have the equivalent of a diode OR to prevent reverse current during faults and hotplug.

Accurate voltage sensing and a programmable turn-off threshold allows operation to be tailored for a wide range of implementations and bus characteristics. The TPS2419 brings out an enable pin which allows the system to force the MOSFET off under light-load, high noise conditions.

Table 1. Family Features

	'2410	'2411	'2412	'2413	'2419
Enable input	√	√			√
Linear gate control	√		√		
ON/OFF gate control		√		√	√
Turnoff comparator filtering	√	√			
Voltage monitoring	√	√			
MOSFET fault monitoring	√	√			
Status pin	√	√			
Independent Supply Pin	√	√	√	√	

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PRODUCT INFORMATION(1)

DEVICE	TEMPERATURE	PACKAGE(1)	MOSFET GATE CONTROL	MARKING
TPS2419	–40°C to 85°C	PW (TSSOP-8)	ON/OFF	2419
		D (SO-8)		2419D

(1) For package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over recommended operating junction temperature range, voltages are referenced to GND (unless otherwise noted)

		VALUE	UNIT
	A, C voltage	–0.3 to 18	V
	A above C voltage	7.5	V
	C above A voltage	18	V
	GATE, BYP voltage(2)	–0.3 to 30	V
	BYP to A voltage	–0.3 to 13	V
	GATE above BYP voltage	0.3	V
	RSET(2) voltage	–0.3 to 7	V
	EN	–0.3 to 5.5	V
	GATE short to A or C or GND	Indefinite	
ESD	Human body model	2	kV
	Charged device model	500	V
T_J	Maximum junction temperature	Internally limited	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Voltage should not be applied to these pins.

DISSIPATION RATINGS

PACKAGE	θ_{JA} – Low k °C/W	θ_{JA} – High k °C/W	POWER RATING High k T_A = 85°C (mW)
PW (TSSOP)	258	159	250
D (SO)	176	97.5	410

RECOMMENDED OPERATING CONDITIONS

voltages are referenced to GND (unless otherwise noted)

		MIN	NOM	MAX	UNIT
A, C	Input voltage range(1)	0		16.5	V
A to C	Operational voltage			5	V
EN	Input voltage range	0		5	V
$R_{(RSET)}$	Resistance range(2)	1.5		∞	kΩ
$C_{(BYP)}$	Capacitance Range(2)	800	2200	10k	pF
T_J	Operating junction temperature	–40		125	°C

(1) $V_{(C)}$ must exceed 2.5 V for normal operation and 3 V to meet gate drive specification
(2) Voltage should not be applied to these pins.

ELECTRICAL CHARACTERISTICS(1)

Common conditions (unless otherwise noted) are: [3 V ≤ ($V_{(A)}$, $V_{(C)}$) ≤ 18 V] , $C_{(BYP)}$ = 2200 pF, $R_{(RSET)}$ = open, EN = 2 V, GATE = open, –40°C ≤ T_J ≤ 125°C, positive currents into pins, typical values are at 25°C, all voltages with respect to GND.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
A, C					
Supply UVLO	$V_{(C)}$ rising	2.25		2.5	V
	Hysteresis		0.25		
A current	| $I_{(A)}$ |, Gate in active region		0.66	1	mA
	| $I_{(A)}$ |, Gate saturated high		0.1		
C current	Worst case, gate in active region, $V_{(AC)}$ ≤ 0.1 V		4.25	6	mA
	Gate saturated high, $V_{(AC)}$ ≤ 0.1 V		1.2		
EN					
Threshold voltage	$V_{(EN)}$ rising	1.25	1.3	1.35	V
Hysteresis			29		mV
Response time	$V_{(AC)}$ = 0.1 V, $V_{(EN)}$↑ : 1.1 V → 1.4 V, measure period to $V_{(GATE)}$ = 0.25 V		0.65	1	µs
	$V_{(AC)}$ = 0.1 V, $V_{(EN)}$↓: 1.4 V → 1.1 V, measure period to $V_{(GATE)}$ = $V_{(ON)}$ - 0.25 V		0.3	0.6	
Leakage current (source or sink)	$V_{(EN)}$ = 0.5 V			1	µA
TURN ON					
Forward turn-on voltage - V_{ON}	$V_{(A-C)}$	58	65	71	mV
TURN OFF					
Turn-off threshold voltage	Gate sinks > 10 mA at $V_{(GATE-A)}$ = 2 V				mV
	$V_{(A-C)}$ falling, $R_{(RSET)}$ = open	1	3	5	
	$V_{(A-C)}$ falling, $R_{(RSET)}$ = 28.7 kΩ	-17	-13.25	-10	
	$V_{(A-C)}$ falling, $R_{(RSET)}$ = 3.24 kΩ	-170	-142	-114	
Turn-off delay	$V_{(A)}$ = 12 V, $V_{(A-C)}$: 20 mV → –20 mV, $V_{(GATE-A)}$ begins to decrease		70		ns
Turn-off time	$V_{(A)}$ = 12 V, $C_{(GATE-GND)}$ = 0.01 µF, $V_{(A-C)}$: 20 mV → –20 mV, measure the period to $V_{(GATE)}$ = $V_{(A)}$		130		ns

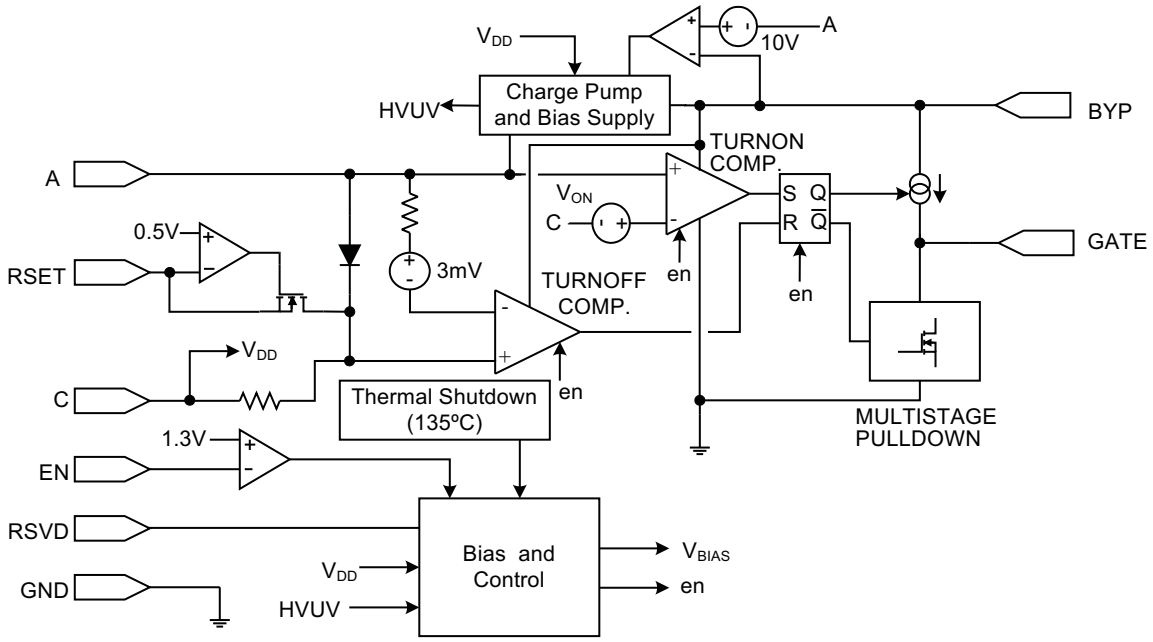
(1) Parameters with only typical values are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

ELECTRICAL CHARACTERISTICS(1) (continued)

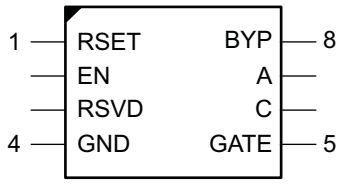
Common conditions (unless otherwise noted) are: [3 V ≤ ($V_{(A)}$, $V_{(C)}$) ≤ 18 V] , $C_{(BYP)}$ = 2200 pF, $R_{(RSET)}$ = open, EN = 2 V, GATE = open, –40°C ≤ T_J ≤ 125°C, positive currents into pins, typical values are at 25°C, all voltages with respect to GND.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GATE					
Gate positive drive voltage, $V_{(GATE-A)}$	$V_{(C)}$ = 3 V, $V_{(A-C)}$ = 200 mV	6	7	8	V
	5 V ≤ V_C ≤ 18 V, $V_{(A-C)}$ = 200 mV	9	10.2	11.5	
Gate source current	$V_{(A-C)}$ = 200 mV, $V_{(GATE-A)}$ = 4 V	250	290	350	µA
Turn-off pulsed current, $I_{(GATE)}$	$V_{(A-C)}$ = –0.1 V				A
	$V_{(GATE)}$ = 8 V	1.75	2.35		
	$V_{(GATE)}$ = 5 V	1.25	1.75		
	Period	7.5	12.5		µs
Sustain turn-off current, $I_{(GATE)}$	$V_{(A-C)}$ = –0.1 V, 3 V ≤ V_C ≤ 18 V, 2 V ≤ $V_{(GATE)}$ ≤ 18 V	15	19.5		mA
MISCELLANEOUS					
Thermal shutdown temperature	Temperature rising, T_J		135		°C
Thermal hysteresis			10		°C

FUNCTIONAL BLOCK DIAGRAM



PW and D PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
RSET	1	I	Connect a resistor to ground to program the turn-off threshold. Leaving RSET open results in a slightly positive $V_{(A-C)}$ turn-off threshold.
EN	2	I	Pull EN above 1.3 V to permit normal ORing operation. A low on EN holds GATE low.
RSVD	3	PWR	This pin must be connected to GND.
GND	4	PWR	Device ground.
GATE	5	O	Connect to the gate of the external MOSFET. Controls the MOSFET to emulate a low forward-voltage diode.
C	6	I	Voltage sense input that connects to the simulated diode cathode, and also serves as the bias supply for the gate drive charge pump and internal controls. Connect to the MOSFET drain in the typical configuration.
A	7	I	Voltage sense input that connects to the simulated diode anode, and also serves as the reference for the charge-pump bias supply on BYP. Connect to the MOSFET source in the typical configuration.
BYP	8	I/O	Connect a capacitor from BYP to A to filter the gate drive supply voltage.

DETAILED DESCRIPTION

The following descriptions refer to the pinout and the functional block diagram.

A, C: The A pin serves as the simulated diode anode and the C as the cathode. GATE is driven high when $V_{(A-C)}$ exceeds 65 mV. A strong GATE pull-down is applied when $V_{(A-C)}$ is less than the programmable turn-off threshold (see RSET). These two thresholds serve as a hysteretic GATE control with the ON/OFF state preserved until the next (opposite) threshold cross.

The internal charge pump output, which provides bias power to the comparators and voltage to drive GATE, is referenced to A. Some charge pump current appears on A.

C is both the cathode voltage sense and the bias supply for the gate-drive charge pump and other internal circuits. This pin must be connected a source that is 3 V or greater when the external MOSFET is to be turned on.

A 0.01-µF minimum bypass capacitor to GND is recommended for both A and C inputs. A and C connections to the bypass capacitor and the controlled MOSFET should be short and low impedance.

The inputs are protected from excess differential voltage by a clamp diode and series resistance. If C falls below A by more than about 0.7 V, a small current flows out of C. Configurations which permit C to be more than 6 V lower than A should be avoided.

BYP: BYP is the internal charge pump output, and the positive supply voltage for internal comparator circuits and GATE driver. A capacitor must be connected from BYP to A. While the capacitor value is not critical, a 2200-pF ceramic is recommended. Traces to this part must be kept short and low impedance to provide adequate filtering. Shorting this pin to a voltage below A damages the TPS2419.

EN: A voltage greater than 1.3 V on EN permits the TPS2419 to operate in its normal ORing mode. A voltage below the lower threshold forces GATE to remain low, however EN going high will not automatically turn GATE ON. EN going low when GATE is high engages the sustain current pulldown. EN should not be driven higher than its recommended maximum voltage.

GATE: Gate controls the external N channel MOSFET gate. GATE is driven positive with respect to A by a driver operating from the voltage on BYP. A time-limited high current discharge source pulls GATE to GND when the turn-off comparator is activated. The high-current discharge is followed by a sustaining pull-down. The turn-off circuits are disabled by the thermal shutdown, leaving a resistive pull-down to keep the gate from floating. The gate connection should be kept low impedance to maximize turn-off current.

GND: This is the input supply reference. GND should have a low impedance connection to the ground plane. It carries several Amperes of rapid-rising discharge current when the external MOSFET is turned off, and also carries significant charge pump currents.

RSET: A resistor connected from this pin to GND sets the $V_{(A-C)}$ turn-off comparator threshold. The threshold is slightly positive when the RSET pin is left open. Current drawn by the resistor programs the turn-off voltage to increasing negative values. The TPS2419 must have a negative threshold programmed to avoid an unstable condition at light load. The expression for $R_{(RSET)}$ in terms of the turn-off voltage ($V_{(OFF)} = V_{(A)} - V_{(C)}$) follows.

$$R_{(RSET)} = \left(\frac{-470.02}{V_{(OFF)} - 0.00314} \right) \quad (1)$$

The units of the numerator are (V × V/A). $V_{(OFF)}$ is positive for $V_{(A)}$ greater than $V_{(C)}$, $V_{(OFF)}$ is less than 3 mV, and $R_{(RSET)}$ is in ohms.

RSVD: Connect to ground.

TYPICAL CHARACTERISTICS

TURNOFF THRESHOLD vs TEMPERATURE

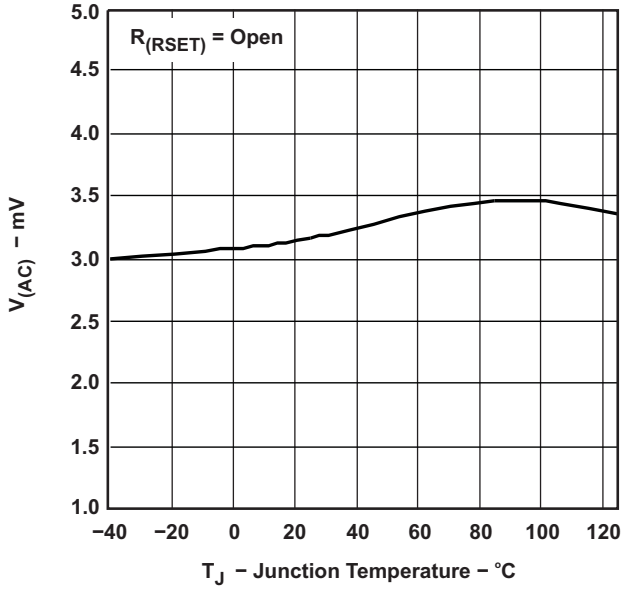


Figure 2.

PULSED GATE SINKING CURRENT vs GATE VOLTAGE

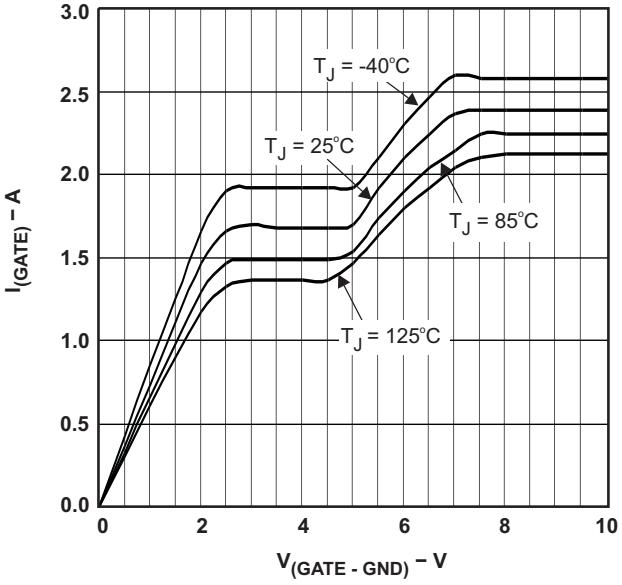


Figure 3.

TURNON DELAY vs $V_{(C)}$ (POWER APPLIED UNTIL GATE IS ACTIVE)

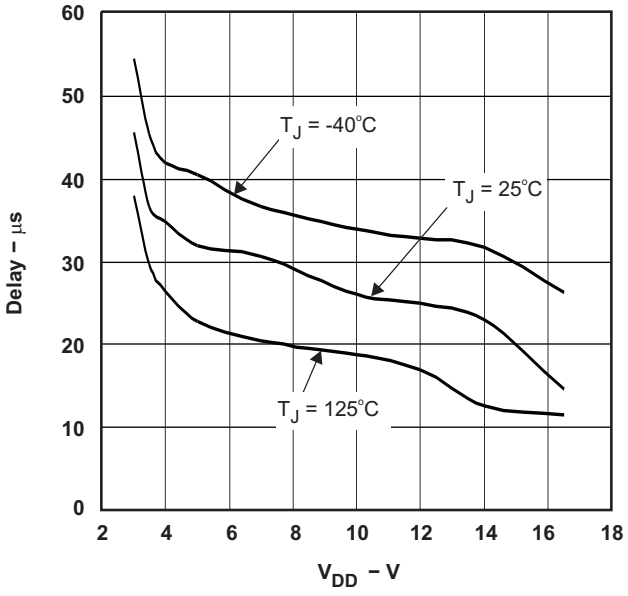


Figure 4.

$I_{(C)}$ vs $V_{(C)}$ (GATE SATURATED HIGH)

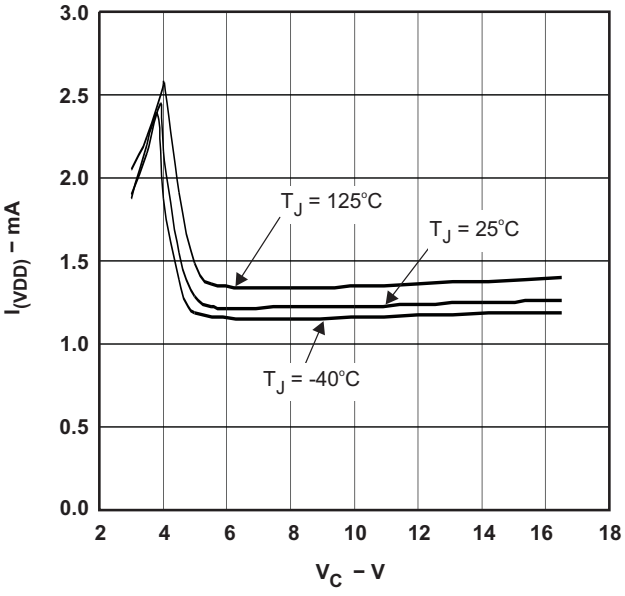


Figure 5.

TYPICAL CHARACTERISTICS (continued)

TURN ON VOLTAGE vs TEMPERATURE

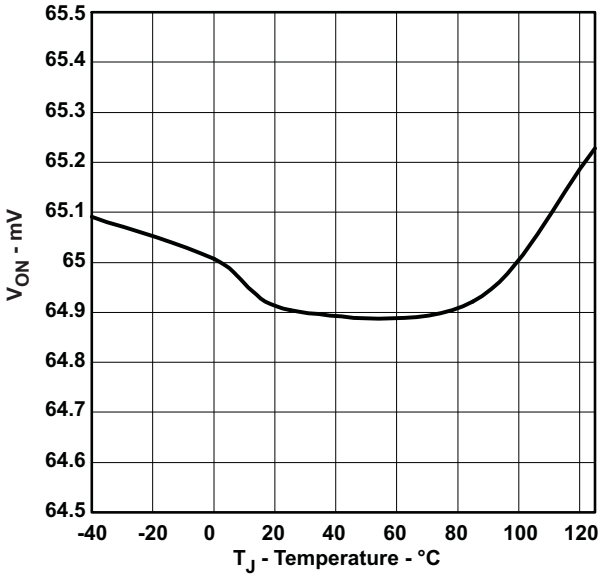


Figure 6.

ENABLETHRESHOLD vs TEMPERATURE

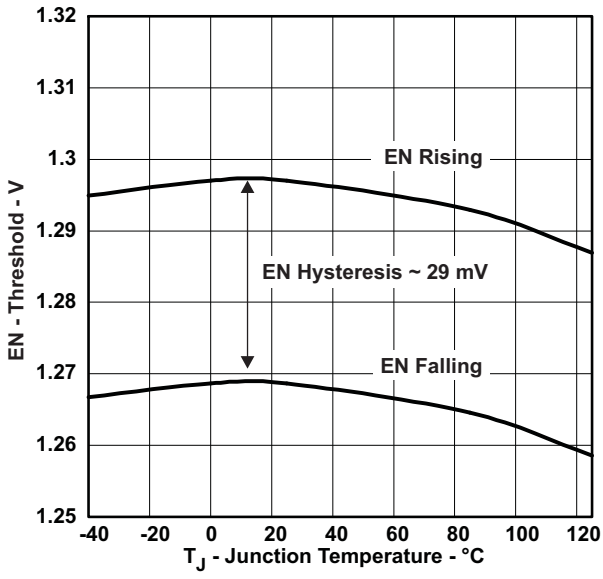


Figure 7.

EXAMPLE TURNON AND TURNOFF

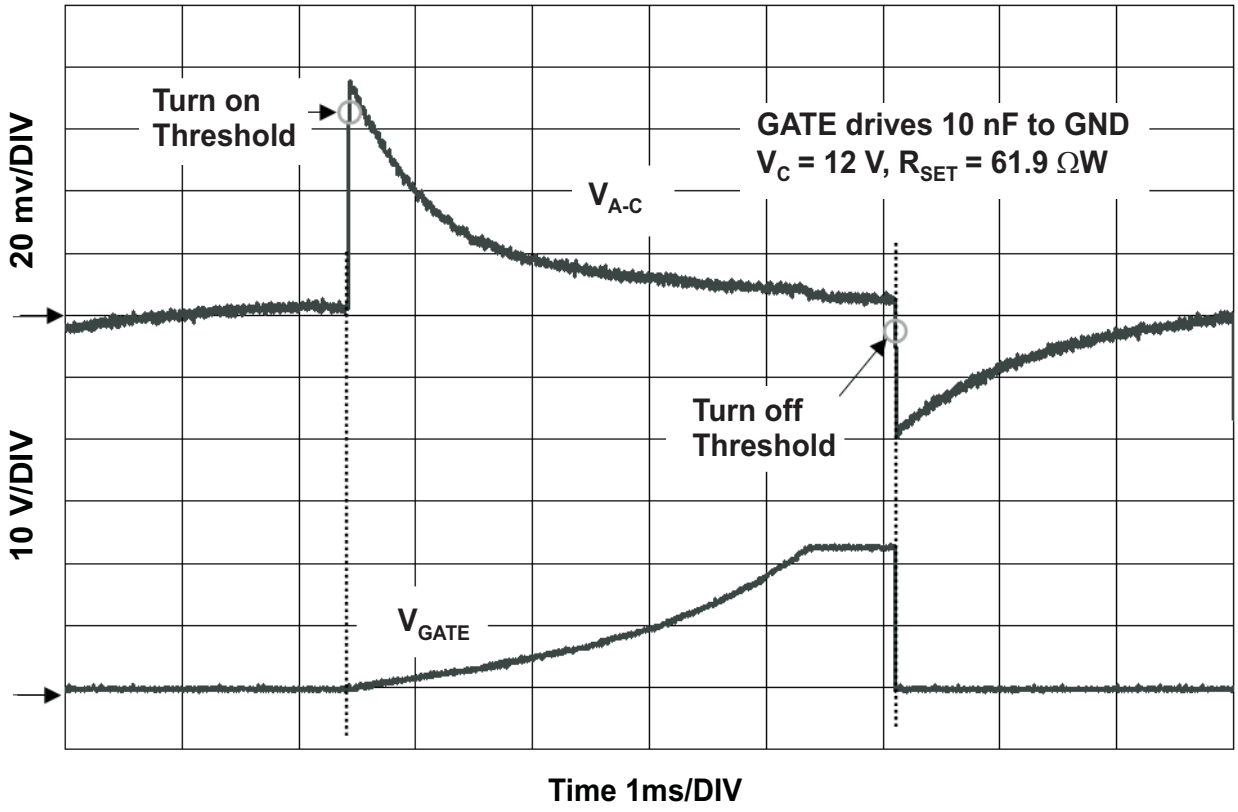


Figure 8.

TYPICAL CHARACTERISTICS (continued)

EXAMPLE TURNOFF

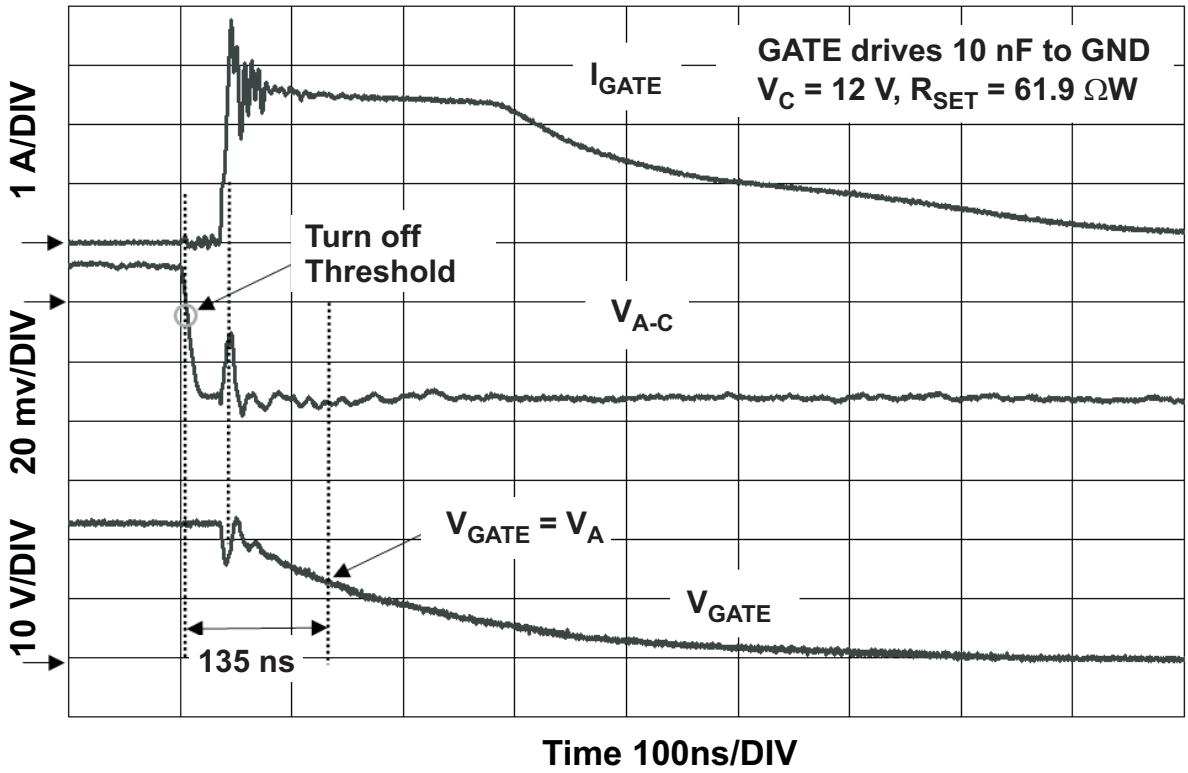


Figure 9.

APPLICATION INFORMATION

OVERVIEW

The TPS2419 is designed to allow an output ORing in N+1 power supply applications (see Figure 11), and an input-power bus ORing in redundant source applications (see Figure 12). The TPS2419 and external MOSFET emulate a discrete diode to perform this unidirectional power combining function. The advantage to this emulation is lower forward voltage drop and higher efficiency.

The TPS2419 turns the MOSFET on and off like a comparator with hysteresis as shown in Figure 10. GATE is driven high when $V_{(A-C)}$ exceeds 65 mV, and driven low if $V_{(A-C)}$ falls below the RSET programmed turn-off threshold. Operation of the TPS2419 is demonstrated in Figure 8 where an ac-coupled square wave is applied from A to C. Figure 8 shows the condition where the MOSFET gate is initially at GND, and $V_{(A-C)}$ is less than 65 mV. When the turn-on threshold is exceeded, the TPS2419 turns on the MOSFET gate, and charges it to $V_{(BYP)}$. The gate stays high even though $V_{(A-C)}$ is less than the turn-on threshold. The TPS2419 pulls the gate to GND when $V_{(A-C)}$ falls below the turn-off threshold.

System designs should account for the inherent delay between a TPS2419 circuit becoming forward biased, and the MOSFET actually turning ON. The delay is the result of the MOSFET gate capacitance charge from ground to its threshold voltage by the 290 µA gate current. If there are no additional sources holding a common ORed rail voltage up, the MOSFET internal diode will conduct and maintain voltage on the ORed output. The ORed input supply will experience a momentary large current draw as the MOSFET turns on, shorting the internal diode and charging the bus capacitance.

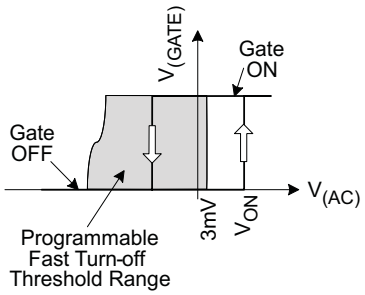


Figure 10. TPS2419 Operation

The operation of the TPS2419 is summarized in Table 2.

Table 2. Operation as a Function of $V_{(AC)}$

	$V_{(A-C)}$ ≤ Turnoff Threshold(1)	Turnoff Threshold(1) ≤ $V_{(A-C)}$ ≤ 65 mV	$V_{(A-C)}$ > 65 mV
TPS2419	Gate pulled to GND	Depends on previous state(1) (Hysteresis region)	GATE pulled high (ON)

(1) Turnoff threshold is established by the value of RSET.

N+1 POWER SUPPLY – TYPICAL CONNECTION

The N+1 power supply configuration shown in Figure 11 is used where multiple power supplies are paralleled for either higher capacity, redundancy or both. If it takes N supplies to power the load, adding an extra identical unit in parallel permits the load to continue operation in the event that any one of the N supplies fails. The supplies are ORed together, rather than directly connected to the bus, to isolate the converter output from the bus when it is plugged-in or fails short. Thus, the TPS2419 with an external MOSFET emulates the function of the ORing diode.

ORed supplies are usually designed to share power by various means, although the desired operation could implement an active and standby concept. Sharing approaches include both passive, or voltage droop, and active methods. Not all of the output ORing devices may be ON depending on the sharing control method, bus loading, distribution resistances, and tolerances.

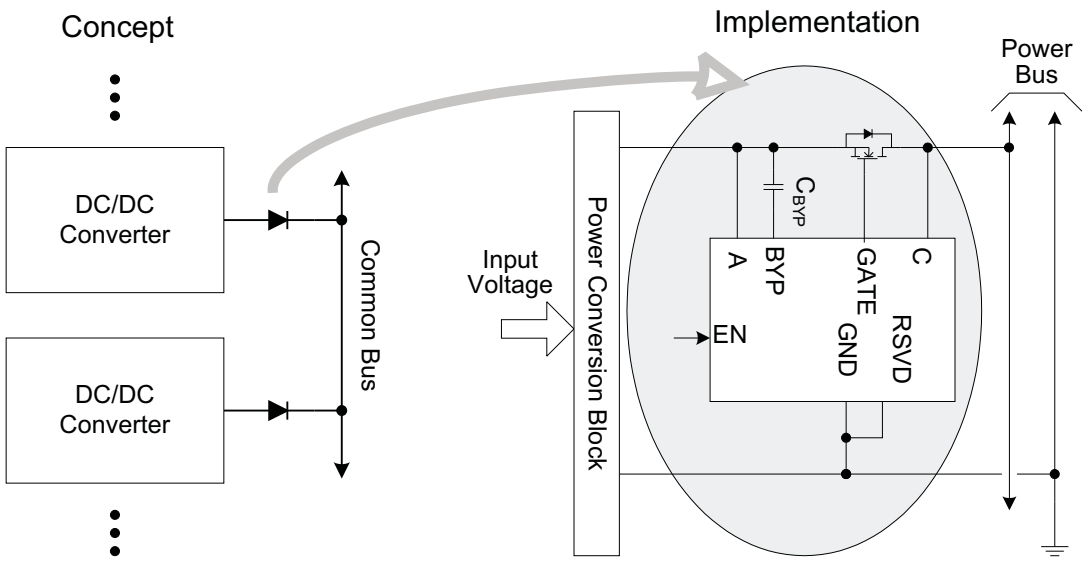


Figure 11. N+1 Power Supply Example

INPUT ORing – TYPICAL CONNECTION

Figure 12 shows how redundant buses may be ORed to a common point to achieve higher reliability. It is possible to have both MOSFETs ON at once if the bus voltages are matched, or the combination of tolerance and regulation causes both TPS2419 circuits to see a forward voltage. The ORing MOSFET will disconnect the lower-voltage bus, protecting the remaining bus from potential overload by a fault.

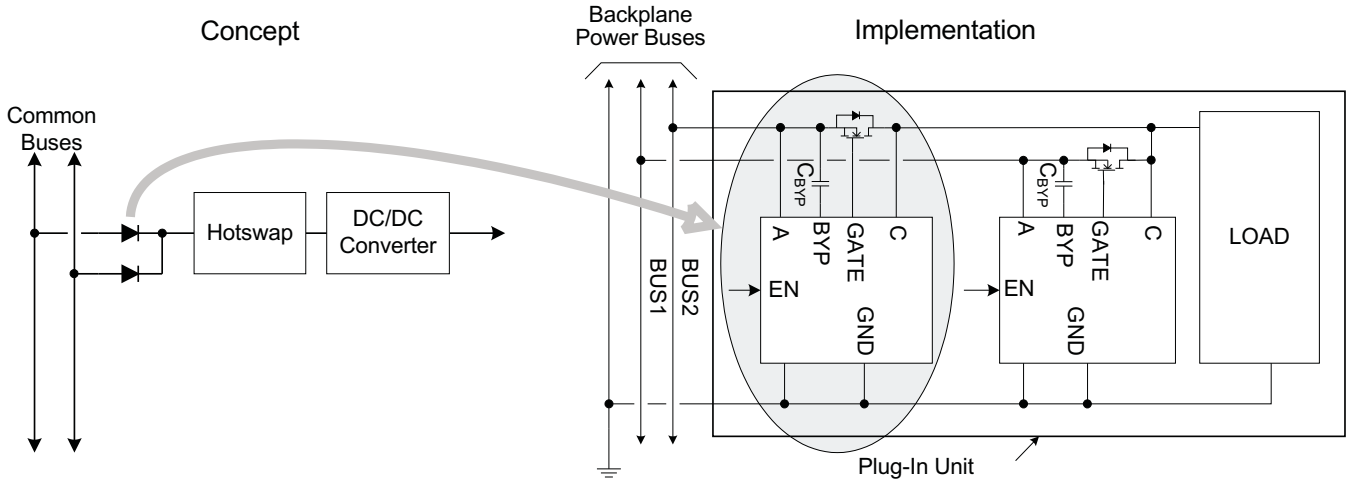


Figure 12. Example ORing of Input Power Buses

SYSTEM DESIGN AND NOISE ISSUES

In noisy system environments, the low impedance of a MOSFET coupled with a default positive turn off threshold voltage might result in unwanted ON/OFF GATE cycling. Ideally the best way to approach the problem is with a clean layout and noise free system design. Since design constraints limit the ability to improve this, the following suggestions can be employed with the TPS2419.

- Set the turn off threshold negative using the RSET pin. This is required to operate at light load, but does permit reverse current.
- If current monitoring is used in the system, take advantage of the shunt resistor and connect the A and C pins across the shunt and FET. This increases the sense resistance, reducing noise sensitivity by increasing the signal levels while reducing the permitted reverse current.
- Disable the device using EN under light load conditions.

RECOMMENDED OPERATING RANGE

The maximum recommended bus voltage is lower than the absolute maximum voltage ratings on A and C, solely to provide some margin for transients on the bus. The TPS2419 will operate properly up to the absolute maximum voltage ratings on A and C.

Most power systems experience transient voltages above or below the normal operating level. Short transients, or voltage spikes, may be clamped by the ORing MOSFET to an output capacitor and/or voltage rail depending on the system design. Protection may be required on the input or output if the system design does not inherently limit transient voltages between the TPS2419 absolute maximum ratings (positive or negative).

Protection for positive transients that would exceed the absolute maximum limits may be accomplished with a TVS diode (transient voltage suppressor) clamp to ground, or a diode clamp to a safe voltage rail. If a TVS is required, it must protect to the absolute maximum ratings at the worst case clamping current. Protection for negative transients that would drive pins (e.g. C) below the absolute maximum limits may be accomplished with a diode clamp to ground. Limit transient current in or out of the TPS2419 to less than 50 mA. Transients can also be controlled by bus capacitance or composite snubber/clamps such as a zener-blocked large capacitor with a discharge resistor in parallel.

MOSFET SELECTION AND $R_{(RSET)}$

MOSFET selection criteria include voltage rating, voltage drop, power dissipation, size, and cost. The voltage rating consists of both the ability to withstand the rail voltage with expected transients, and the gate breakdown voltage. The MOSFET gate rating should exceed be the maximum of the controlled rail voltage or 11.5 V.

While $r_{DS(on)}$ is often chosen with the power dissipation, voltage drop, size and cost in mind, there are several other factors to be concerned with in ORing applications. When using a TPS2419 with RSET programmed to a negative voltage, the permitted static reverse current is equal to the turn-off threshold divided by the MOSFET's $r_{DS(on)}$. While this current may actually be desirable in some systems, the amount may be controlled by selection of $r_{DS(on)}$ and RSET. The practical range of $r_{DS(on)}$ for a single MOSFET runs from the low milliohms to 40 mΩ for a single MOSFET.

MOSFETs may be paralleled for lower voltage drop (power loss) at high current. Current sharing depends on the resistance match including both the $r_{DS(on)}$, connection resistance, and thermal coupling.

The TPS2419 may only be operated without an RSET programming resistor if the loading provides a $V_{(A-C)}$ greater than 3 mV. A negative turnoff threshold reduces sensitivity to false tripping due to noise on the bus, but permits larger static reverse current. Installing a resistor from RSET to ground creates a negative shift in the turn-off threshold per Equation 2.

$$R_{(RSET)} = \left(\frac{-470.02}{V_{(OFF)} - 0.00314} \right) \quad (2)$$

To obtain a -10 mV turnoff ($V_{(A)}$ is less than $V_{(C)}$ by 10 mV), $R_{(RSET)}$ = (–470.02/ (–0.01–0.00314)) ≈ 35.7 kΩ. If a 10 mΩ $r_{DS(on)}$ MOSFET was used, the reverse turnoff current would be calculated as follows.

$$I_{(TURN\_OFF)} = \frac{V_{(THRESHOLD)}}{r_{DS(on)}}$$

$$I_{(TURN\_OFF)} = \frac{-10\ mV}{10\ m\Omega}$$

$$I_{(TURN\_OFF)} = -1\ A \quad (3)$$

The sign indicates that the current is reverse, or flows from the MOSFET drain to source (C to A).

The turn-off speed of a MOSFET is influenced by the effective gate-source and gate-drain capacitance C_{ISS}). Since these capacitances vary a great deal between different vendor parts and technologies, they should be considered when selecting a MOSFET where the fastest turn-off is desired.

GATE DRIVE, CHARGE PUMP AND $C_{(BYP)}$

Gate drive of 290 µA typical is generated by an internal charge pump and current limiter. Make sure to use low impedance traces and good bypass on A and C to avoid having the large charge pump currents interfere with voltage sensing. The GATE drive voltage is referenced to $V_{(A)}$ as GATE will only be driven high when $V_{(A)} > V_{(C)}$. The capacitor on BYP (bypass) must be used in order to form a quiet supply for the internal high-speed comparator.

Gate Drive Resistance and Output Transients

The strong gate (pulsed) pull-down current can turn the ORing MOSFET(s) off in the 100 - 200 ns time frame. While this serves to rapidly stop the reverse current buildup, it has a side effect of inducing a voltage transient on the input bus, the output bus, and ground. One transient source is the GATE turn-off current itself, which excites parasitic L-C tank circuits. A second transient source is the energy stored in power bus inductance driving a voltage surge and ringing as reverse MOSFET current is interrupted. Both of these effects can be reduced by limiting the GATE discharge current with a series resistor in the 10 Ω to 200 Ω range. This both reduces the peak discharge current, and slows the MOSFET turnoff, reducing the di/dt. A careful tradeoff of peak reverse current and the effects of the voltage transient may be required.

An example of turnoff speed with and without GATE resistance is illustrated by the circuit of Figure 13. Figure 14 and Figure 15 show GATE, the MOSFET gate, and $V_{C\text{-}ac}$ for similar turnoff transients and gate resistors of 0 Ω and 51 Ω. A substancial reduction in noise is shown for a difference of 90ns in actual current termination. These techniques may be used in conjunction with clamping and snubbing techniques discussed in RECOMMENDED OPERATING RANGE. Figure 13 also demonstrates the filtering discussed in the next section.

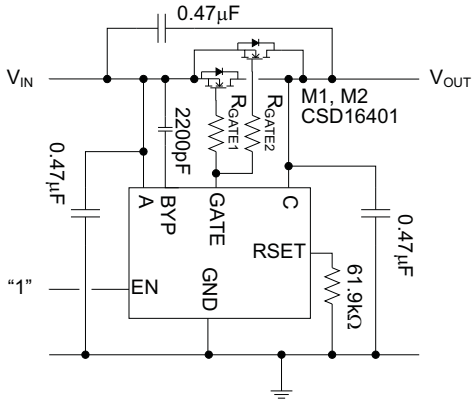


Figure 13. Circuit for Gate Resistor Waveforms

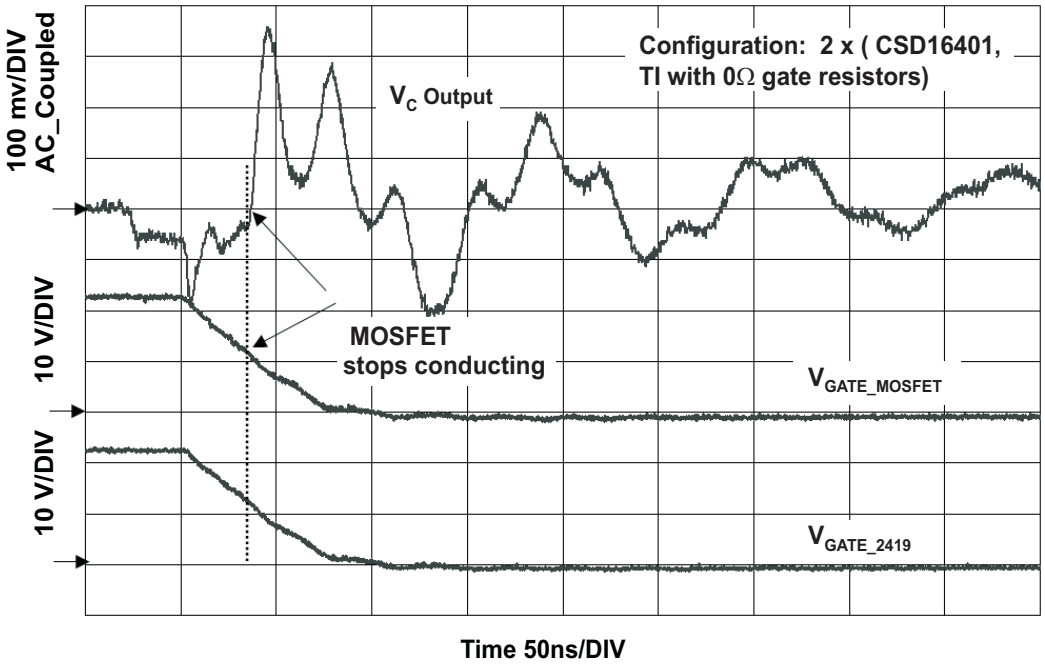


Figure 14. Gate Turnoff Waveforms with R_{GATE} = 0Ω

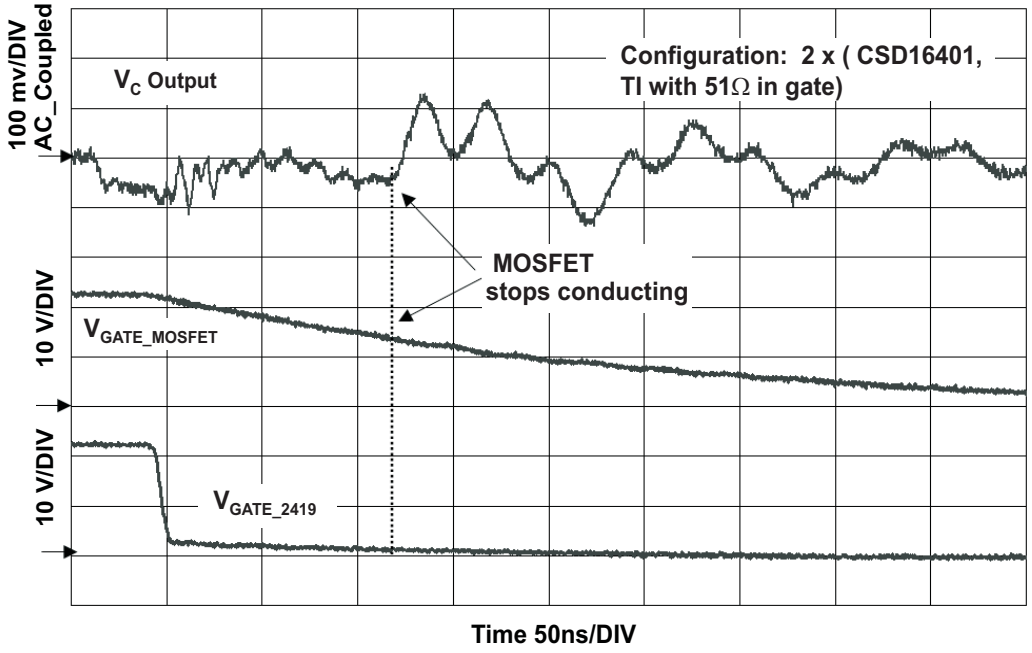


Figure 15. Gate Turnoff Waveforms with R_{GATE} = 51Ω

Input Filtering

Voltage transients, converter switching noise and ripple, and ringing due to current interruptions can potentially cause undesired on-off cycling, especially at very light loads. This includes voltage gradients (especially at MHz frequencies) across the ground plane effecting the apparent $V_{(A)}$ and $V_{(C)}$. The effects of these unwanted signals can be reduced by providing input filtering as shown in Figure 16 and Figure 13. There are two potential problems that the filter might have to help with, 1) internally generated switching noise, and 2) fast ringing transients caused by nearby power system events. Case 2 (in Figure 16) filtering is better at suppressing internal switching noise and Case 1 is better for large bus transients in the megahertz range. The "Z" element in CASE 1 is a high-impedance ferrite bead with low resistance to limit the dc voltage error. The L-C filter limits the apparent $V_{(A)}$ voltage swings during high-speed transients. The L-C in series with A also causes a phase delay in sensed steady-state switching noise, creating an apparent additional $V_{(AC)}$.

The filter capacitors should be located close to the TPS2419's GND pin and be connected to GND by a solid plane. The A-C capacitor should be located directly across the TPS2419 pins. These values were empirically chosen in a particular test setup and may have to be tuned for different systems.

The waveform of Figure 17 shows turnon in the presence of 135 mVpp ripple by the circuit of Figure 13. The ORing circuit was loaded with 10 kΩ parallel to 0.1 µF, and had only a -4.5 mV turnoff threshold. This condition is often difficult to turn on into due to the $V_{(A-C)}$ difference that occurs when the MOSFET diode peak charges the output. The output voltage was monitored with the oscilloscope probe ac-coupled, causing visual artifacts due to the probe settling time. The increase in output ripple is evident as the dynamic impedance of the MOSFET diode is shorted by the channel resistance.

Selection of the A and C sense points can also play a role in limiting unwanted turnoff events. Sensing voltages at bus bypass capacitors may benefit operation by limiting the apparent switching and transient noise.

The TPS2419 uses C as both a voltage sense and power pin. Placing resistance in this lead will cause a reduction in $V_{(C)}$ due to IxR voltage drop, changing the apparent turnon and turnoff thresholds.

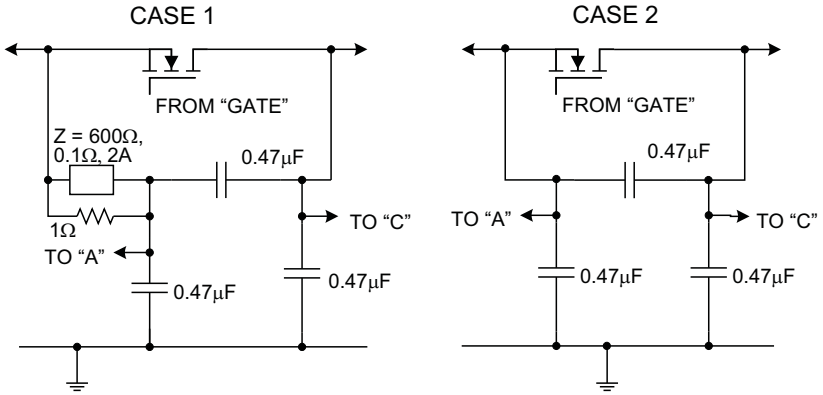


Figure 16. Input Filtering Configurations

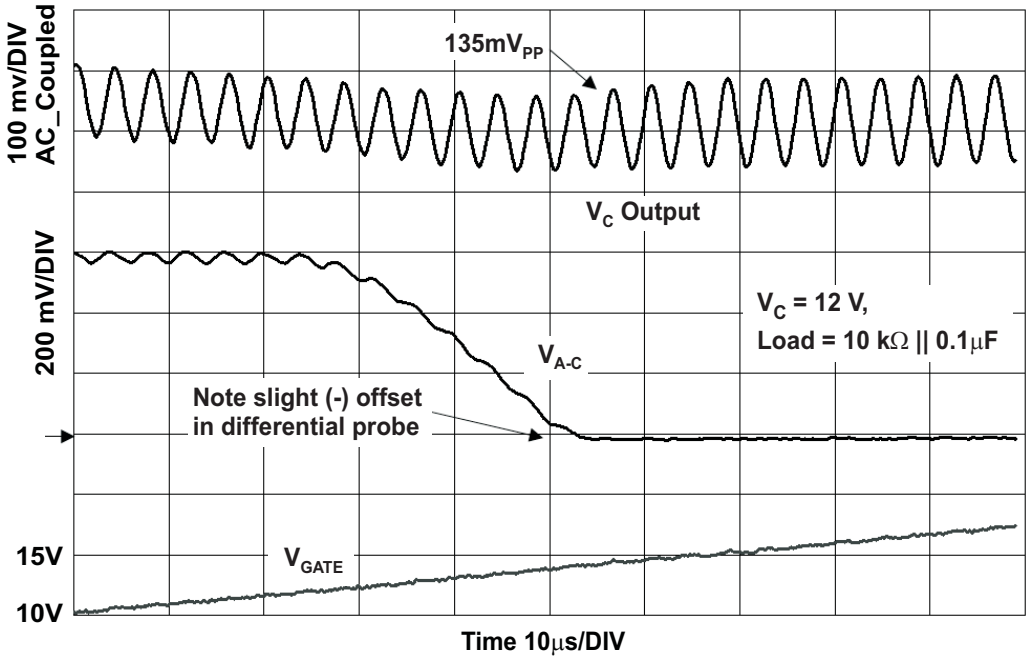


Figure 17. Turnon with Noisy Power Rail

SUMMARIZED DESIGN PROCEDURE

The following is a summarized design procedure:

1. Noise voltage and impedance at the A and C pins should be kept low. A minimum 0.01 µF or more may be required.
2. Select $C_{(BYP)}$ as 2200 pF, X7R, 25-V or 50-V ceramic capacitor.
3. Select the MOSFET based on considerations of voltage drop, power dissipated, voltage ratings, and gate capacitance. See sections: MOSFET Selection and RSET.
4. Select $R_{(RSET)}$ based on which MOSFET was chosen and reverse current considerations – see MOSFET Selection and RSET.
5. Make sure to connect RSVD to ground

Layout Considerations

1. The TPS2419, MOSFET, and associated components should be used over a ground plane.
2. The GND connection should be short and wide, with multiple vias to ground.
3. A and C bypass capacitors should be adjacent to the pins with a minimal ground connection length to the plane.
4. The GATE connection should be short and wide (e.g., 0.025" minimum).
5. Route the A and C sense lines away from noisy sources, and avoid large ground bounce between the MOSFET and TPS2419.
6. $R_{(SET)}$ should be kept immediately adjacent to the TPS2419 with short leads.
7. $C_{(BYP)}$ should be kept immediately adjacent to the TPS2419 with short leads.

REVISION HISTORY

Changes from Original (February 2010) to Revision A **Page**

- Changed the data sheet From: Preview To: Production Data 1
- Changed the Overview section - paragraph 2 From: MOSFET gate is initially low, and $V_{(AC)}$ is less than 64 mV. To: MOSFET gate is initially at GND, and $V_{(A-C)}$ is less than 65 mV. 10
- Changed the Overview section - paragraph 2, From: The TPS2419 turns on the MOSFET gate, and charges it to $V_{(BYP)}$ once the turn-on threshold is exceeded. To: When the turn-on threshold is exceeded, the TPS2419 turns on the MOSFET gate, and charges it to $V_{(BYP)}$ 10
- Changed the Overview section - paragraph 3 From: The ORed input supply will experience a momentary large load as the MOSFET turns on, shorting the internal diode and charging the bus capacitance. To: The ORed input supply will experience a momentary large current draw as the MOSFET turns on, shorting the internal diode and charging the bus capacitance. 10
- Changed the RECOMMENDED OPERATING RANGE section, paragraph 1 From: The TPS2419 will operate properly up to the absolute maximum voltage ratings on A, C, and V_{DD}. To: The TPS2419 will operate properly up to the absolute maximum voltage ratings on A and C. 12

Changes from Revision A (March 2010) to Revision B **Page**

- Added updated marking information 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2419D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2419D	Samples
TPS2419DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2419D	Samples
TPS2419PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2419	Samples
TPS2419PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2419	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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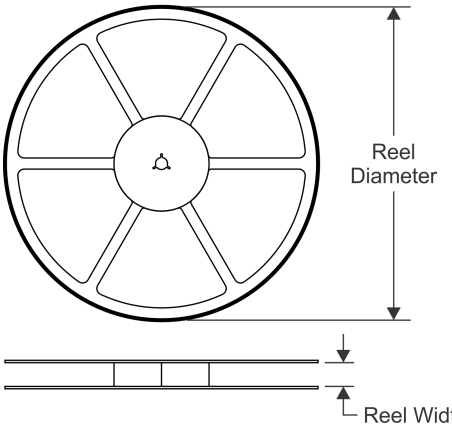
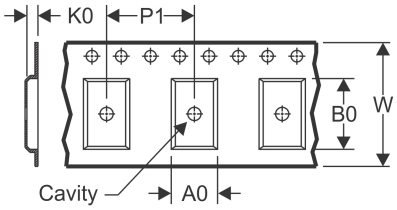
TAPE AND REEL INFORMATION

REEL DIMENSIONS

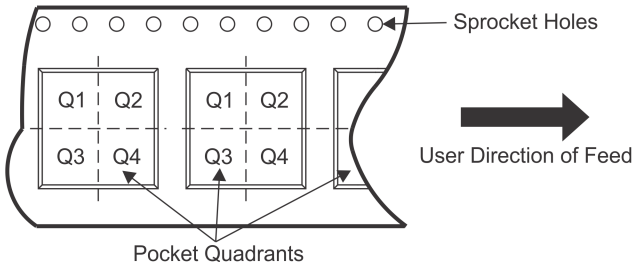


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

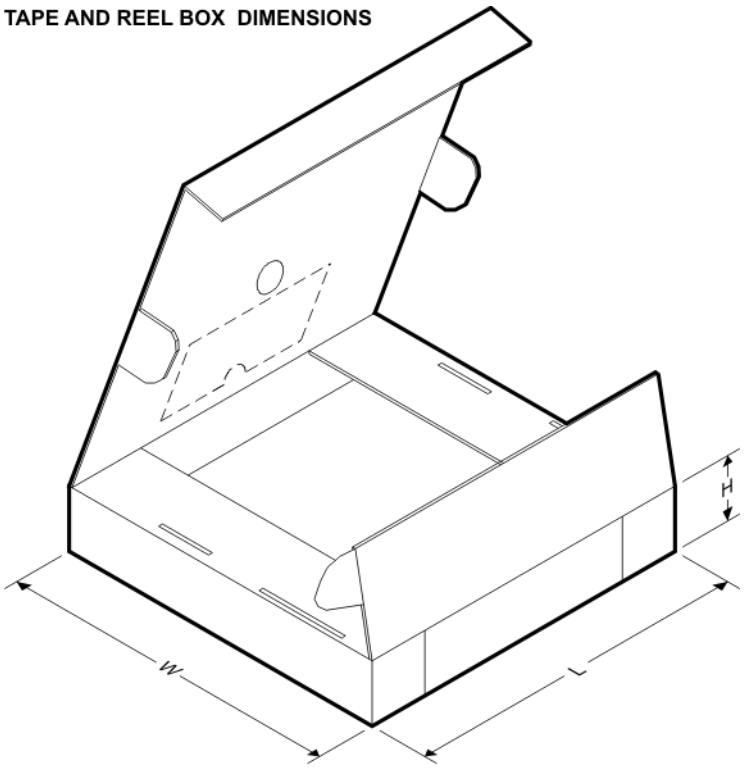
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2419DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2419PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

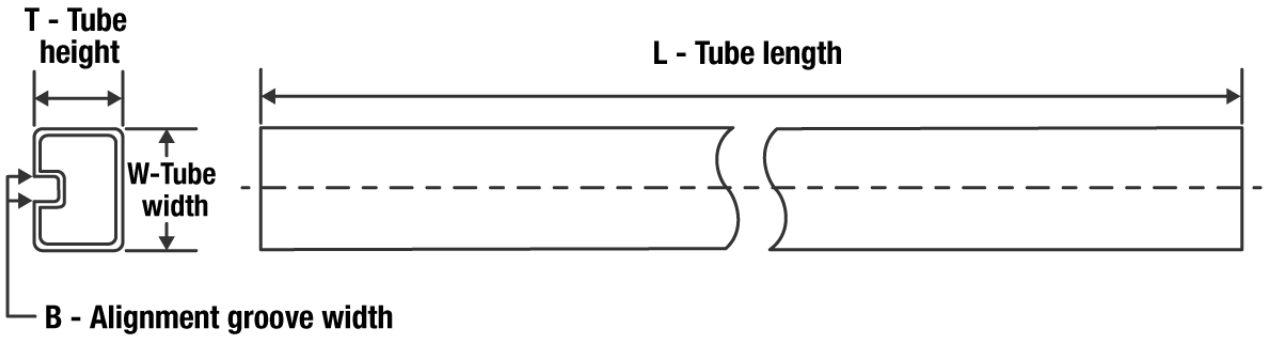
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

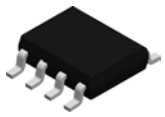
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2419DR	SOIC	D	8	2500	340.5	336.1	25.0
TPS2419PWR	TSSOP	PW	8	2000	853.0	449.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2419D	D	SOIC	8	75	507	8	3940	4.32
TPS2419PW	PW	TSSOP	8	150	530	10.2	3600	3.5

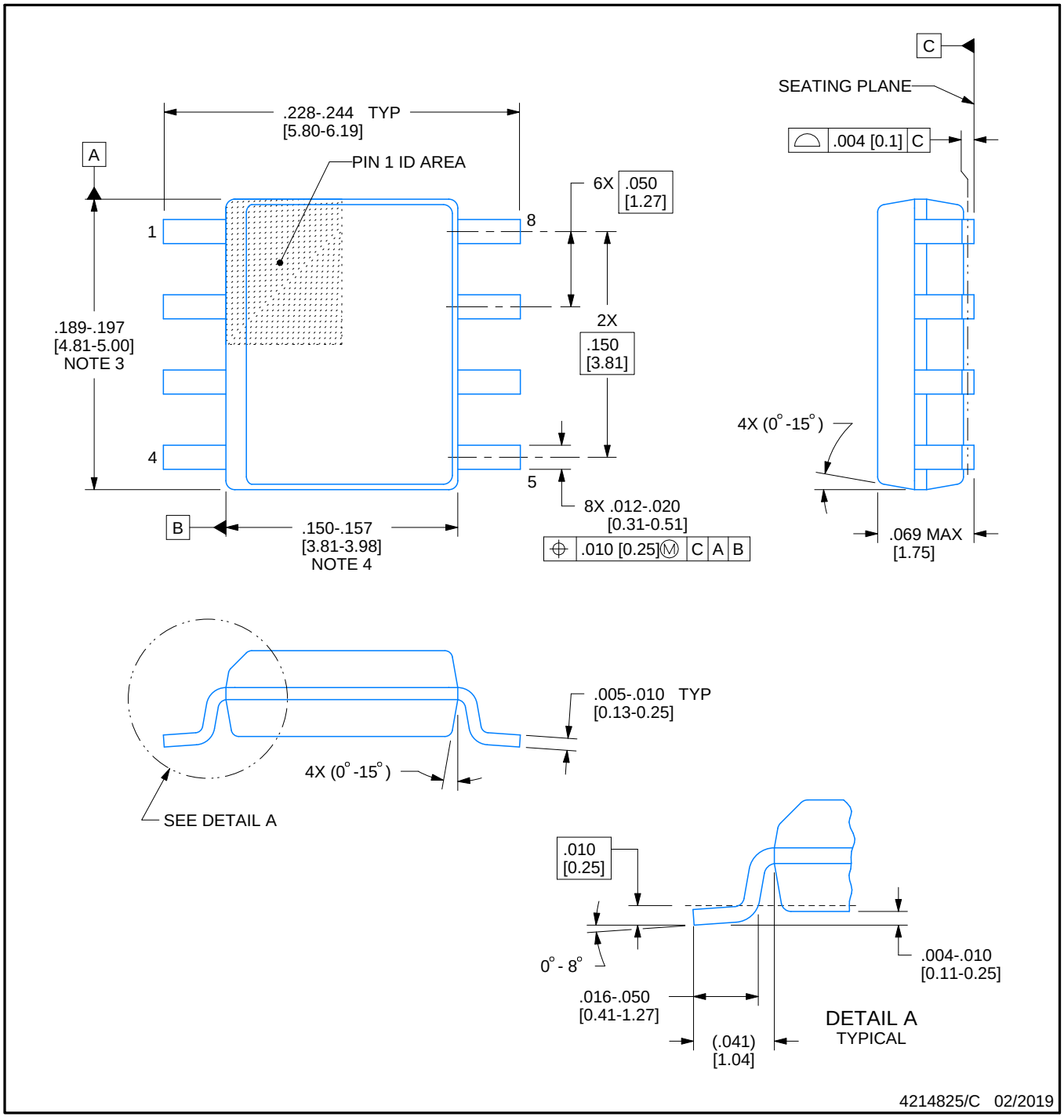


PACKAGE OUTLINE

D0008A

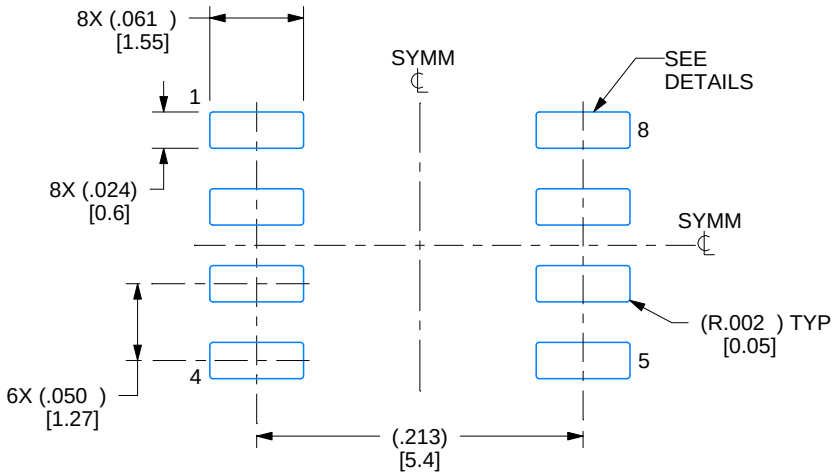
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

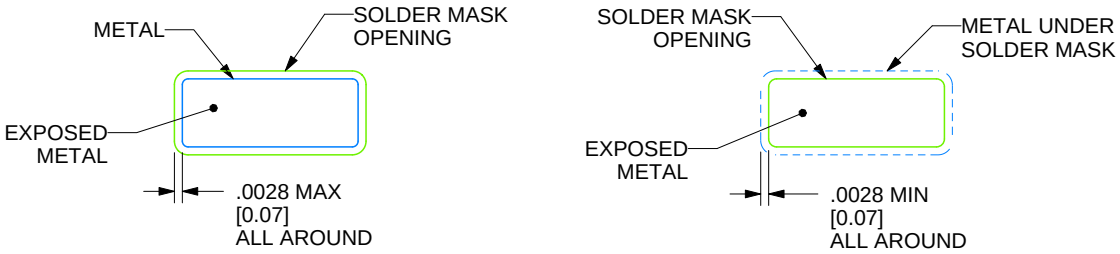


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

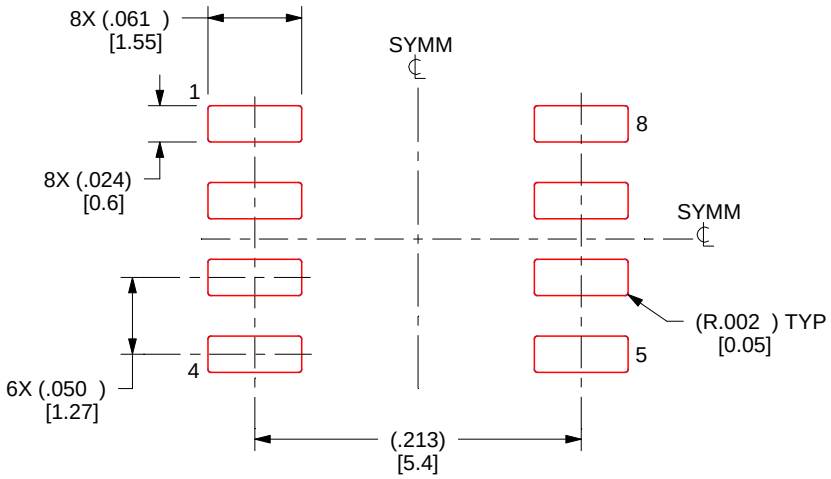
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

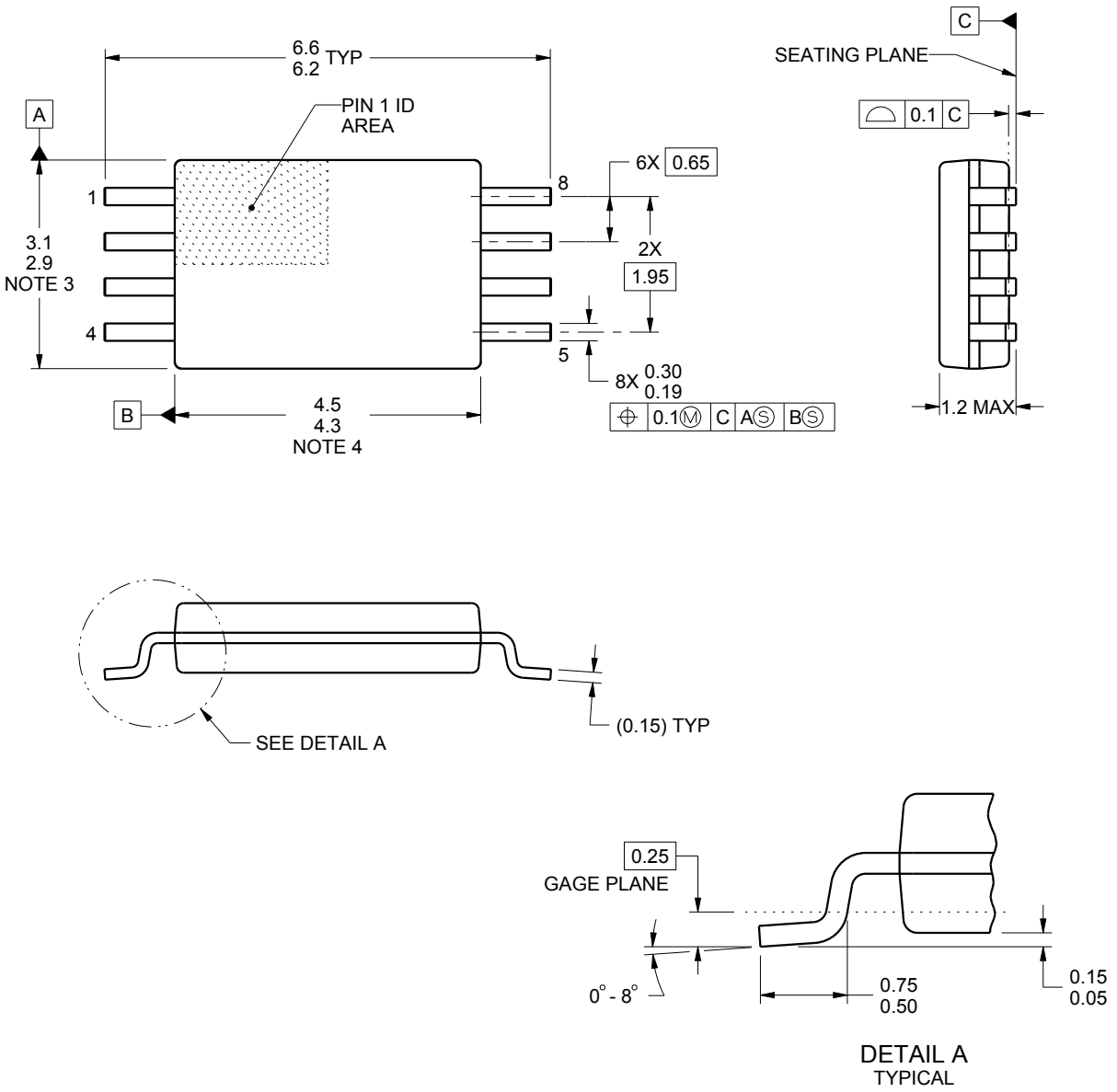
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

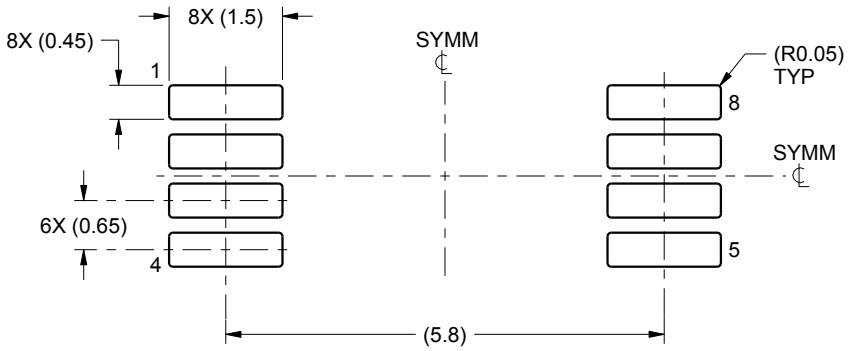
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

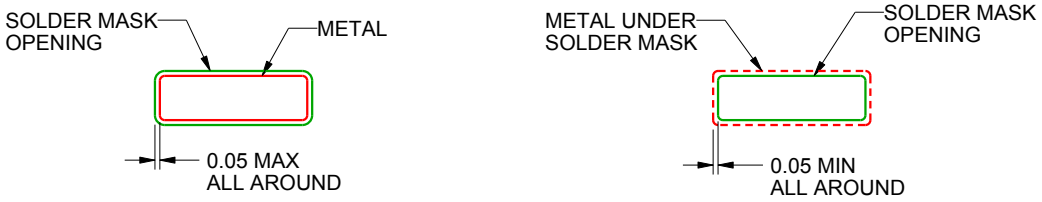


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

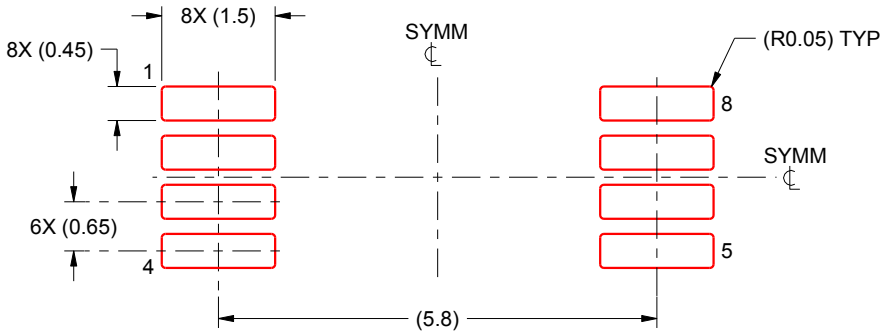


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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