

## Errata

The following are known problems with Rev. C of the AT89LP2052/LP4052 device:

### 1. JBC to TF0, TF1, IE0, IE1, RI, TI

JBC may cause a loss of interrupt information if used with any interrupt flag. Therefore JBC should not be used to poll for interrupt flags.

#### Problem Fix/Workaround:

```
POLL:  JBC FLAG, NEXT
        SJMP POLL
```

#### should be replaced by:

```
POLL:  JNB FLAG, POLL
        CLR FLAG
        SJMP NEXT
```

### 2. Read-Modify-Write to ACSR (ANL, ORL, XRL)

Read-Modify-Write (RMW) instructions may cause a loss of Comparator interrupt information if used with any bit in ACSR, i.e. the RMW instructions need to be treated as a direct move to ACSR such as MOV ACSR,#IMM. These instructions may be used when it is not possible for the interrupt to occur at the same time as the instruction is being executed, which means in the following circumstances:

- A. The Comparator is not active, **or**
- B. Within a short period of time after CF is set, **or**
- C. The flag is level-sensitive and the input condition will last through the next instruction, **or**
- D. Any time if the application can afford to miss an edge event. The actual miss frequency will depend on the application code.

### 3. Read-Modify-Write to TCON (SETB, CLR, CPL, ANL, ORL, XRL)

Read-Modify-Write instructions may cause a loss of external interrupt information if used with TCON. These instructions may be used when it is not possible for the external interrupt to occur at the same time as the instruction is being executed, which means in the following circumstances:

- A. Any time if not using external interrupts or if the interrupts are level sensitive, **or**
- B. If using a single edge-triggered interrupt, within a short time after the flag is set, **or**
- C. Any time if the application can afford to miss an edge event. The actual miss frequency will depend on the application code.

### 3. Interrupt Recovery from Power-down Mode

When attempting interrupt recovery from power-down, the external interrupt pins  $\overline{\text{INT0}}$  (P3.2) and  $\overline{\text{INT1}}$  (P3.3) should not transition low until at least 10  $\mu\text{s}$  after entry into power-down. If the pins are low immediately before entering power-down, or go low while attempting to enter power-down, the device can get stuck in a power-down-like state requiring a power cycling sequence to wake up.



**AT89**  
**Microcontrollers**

**AT89LP2052**  
**AT89LP4052**  
**Rev. C**  
**Errata Sheet**





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