PCN Number:	20140421000	**PCN Date:**	04/28/2014
Title:	DRA64x/65x/AM387x/DM8127/DM814x /TDA1Mx datasheet		
Customer Contact:	PCN Manager	**Phone:** +1(214) 480-6037	**Dept:** Quality Services

Change Type:

☐	Assembly Site	☐	Design	☐	Wafer Bump Site
☐	Assembly Process	☒	Data Sheet	☐	Wafer Bump Material
☐	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

PCN Details

Description of Change:

The product datasheet(s) is being updated:

Applicable updates have been made including:
- Updated/Changed Power-Up Sequence
- Updated/Changed Power-Down Sequence
- Added Automotive POH Profile Table to Absolute Maximum Ratings
- Added Latch-Up Performance Absolute Maximum Ratings
- Low-end OPP combinations no longer supported (CVDD_x < CVDD)

The following change history provides further details. These changes may be reviewed at the datasheet links provided

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

This data manual revision history highlights the technical changes made to the SPRS647D device-specific data manual to make it an SPRS647E revision.

Scope: Applicable updates to the DM814x DaVinci™ Video DMP device family, specifically relating to the TMS320DM8148/47 devices (Silicon Revisions 3.0, 2.1), which are now in the production data (PD) stage of development have been incorporated.

- Updated/Changed Power-Up Sequence
- Updated/Changed Power-Down Sequence
- Low-end OPP combinations no longer supported (CVDD_x < CVDD)
- Added RXACTIVE Function (Bit 18) to PINCTRLx Register Description
- Added Power-On Hours (POH) section
- Added Latch-Up Performance Absolute Maximum Ratings
- DDR2/DDR3 supports up to 533 MHz
- OPP50 is **not** supported
- SmartReflex™ (AVS) is **not** supported
- Deep Sleep Mode is **not** supported
- HDMI HDCP encryption is **not** supported

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Global	• Replaced all instances of "DSP/EDMA MMU" with "**System MMU**" • Deleted all references to OPP50 and Deep Sleep Mode • Deleted the TMS320DM8146 device along with any device-specific information; no longer supported
Section 1 Features	• Updated/Changed description the HD Video Processing Subsystem (HDVPSS) • Updated/Changed the Dual 32-Bit DDR2/DDR3 SDRAM Interfaces sub-bullet from "Supports up to DDR2-800 and DDR3-**800**" to "Supports up to DDR2-800 and DDR3-**1066**"
Section 2.2 Device Characteristics	Table 2-2, Characteristics of the Processor: • Updated/Changed the HD Video Processing Subsystem (HDVPSS) row • Updated/Changed Core Logic (V), OPP100, OPP120 range from "0.95 V – 1.20 V" to "1.10 V – 1.20 V"
Section 2.12.4.2 L4 Slow Peripheral Memory Map	Table 2-7, L4 Slow Peripheral Memory Map: • Updated/Changed 0x4818_8000–0x4818_BFFF Device Name from "SmartReflex0/1 Peripheral and Support Registers" to **"Reserved"** • Updated/Changed 0x4819_0000–0x4819_3FFF Device Name from "SmartReflex2/3 Peripheral and Support Registers" to **"Reserved"**
Section 3.2.7 General-Purpose Input/Outputs (GPIOs)	Table 3-11, GP1 Terminal Functions: • Added "The ENLVCMOS bit in the MLBP_DAT_IO_CTRL register...." to the pin descriptions for pins GP1[10:7] (V2, V1, W2, and W1 respectively).
Section 3.2.25 Reserved Pins	Table 3-48, Reserved Terminal Functions: • Updated/Changed TYPE for Signal No. Y14 (RSV4) and AC8 (RSV5) from "S" to **"I"**

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Section 4 Device Configurations	Section 4.3, Pin Multiplexing Control: • Updated/Changed bit 18 from "RSV" to "RXACTIVE"
	Table 4-11, PINCNTL1 – PINCNTL270 (PINCNTLx) Registers Bit Descriptions: • Updated/Changed the MUXMODE[7:0] Description from "Values other than those ..." to **"A value of zero results ..."** • Updated/Changed bit 18 description to now support RXACTIVE
	Table 4-13, PINCNTLx Registers MUXMODE Functions: • Updated/Changed PINCNTL173 row under 0x20 from "UART2_TXD$^{(M1)}$" to **"UART2_TXD$^{(M0)}$"** • Updated/Changed PINCNTL231 under 0x80 from "GP3[30]$^{(M0)}$" to **"GP3[30]$^{(M1)}$"**
	Section 4.4, Handling Unused Pins: • Added "Unless otherwise noted" to the beginning of, "All supply pins must always ..."
Section 6 Device Operating Conditions	Section 6.1, Absolute Maximum Ratings: • Deleted the "V I/O...(Transient Overshoot/Undershoot)" rows of Input and Output voltage ranges • Added Latch-Up Performance row and Latch-Up footnotes • Updated/Changed ESD-HBM footnote to "Level listed is passing level per ANSI/ESDA/JEDEC J5-001..." • Updated/Changed ESD-CDM footnote to "Level listed is passing level per EIA-JEDEC JESD22-C101E..."
	Section 6.3, Power on Hours (POH): • Added Power-On Hour (POH) section **[New]**
Section 7.2.2.1 Dynamic Voltage Frequency Scaling (DVFS)	Table 7-5, Supported OPP Combinations: • Deleted lower-end OPP combinations supported for ARM, DSP, and HDVICP2
Section 7.2.8.1 Power-Up Sequence	Table 7-6 , Power-Up Sequence Ramping Values: • Added NO. 1 MIN value of "0" ms. • Updated/Changed NO. 1 description to "1.8 V and DVDD_DDR[x] supplies stable..." • Added NO. 13, "CVDD variable supply ramp...." • Updated/Changed Figure 7-1 according to table changes • Deleted 3.3 V Supplies Rising Before 1.8 V Supplies Delta Figure (was Figure 7.2) and associated footnote references • Deleted footnote, "The 3.3 V supplies must be..."
Section 7.2.8.2 Power-Down Sequence	Section 7.2.8.2, Power-Down Sequence: • Added, "Ramping down all supplies at the same time...For proper device..." paragraph
	Table 7-7, Power-Down Sequence Ramping Values: • Updated/Changed "The 1.5-/1.8-V DVDD_DDR[x]..." footnote • Updated/Changed figure reference to Figure 7-3 • Added NO. 14, "CVDD_x variable supplies ramp-down..." • Added associated footnote, "CVDD_x must never exceed CVDD by more than 150mV"
	Figure 7-2, Power-Down Sequence: • Updated/Changed figure according to table changes
	Figure 7-3,1.8 V Supplies Falling Before 3.3 V Supplies Delta: • Added figure **[New]**

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Section 7.4 Clocking	Section 7.4.1.1, Using the Internal Oscillators: Table 7-11, Requirements for Crystal Circuit on the Device Oscillator (DEVOSC): • Added three conditions and the MAX values to the Crystal Frequency Stability PARAMETER
	Table 7-15, Timing Requirements for DEVOSC_MXI/DEV_CLKIN • Added three conditions and the MAX values to the Frequency Stability PARAMETER
	Section 7.4.3, AUD_CLKINx Input Clocks: • Added section **[New]**
	Section 7.4.4, CLKIN32 Input Clock: • Added "/8" to the TIMER1/2/3/4/5/6/7 bullet
	Section 7.4.7, Input/Output Clocks Electrical Data/Timing: • Added Table 7-17, Timing Requirements for AUD_CLKINx **[New]** • Added Figure 7-14, AUD_CLKINx Timing **[New]**
	Section 7.4.8, PLLs: • Deleted PLL Electrical Data/Timing subsection
Section 7.4.9 SYSCLKs	Table 7-26, Maximum SYSCLK Clock Frequencies: • Added footnote, "The maximum frequencies listed..."
Section 7.4.10 Module Clocks	Table 7-27, Maximum Module Clock Frequencies: • Updated/Changed Media Controller **CLOCK SOURCES** from "PLL_MEDIACTL" to "PLL_MEDIACTL/2" • Updated/Changed Media Controller **MAX FREQUENCY OPP100 (MHz)** value from "400" to "200" • Added footnote, "The maximum frequencies listed..."
Section 8.4 EDMA	Section 8.4.1, EDMA Channel Synchronization Events: • Updated/Changed paragraphs
	Section 8.4.2, EDMA Peripheral Register Descriptions: • Added Table 8-5, EDMA Channel Controller (EDMA TPCC) Control Registers • Added Table 8-6, EDMA Transfer Controller (EDMA TPTC) Control Registers
Section 8.5.3 IEEE 1149.1 JTAG	Table 8-8, JTAG ID Register Table: • Added silicon-revision specific information to the VARIANT bit field
Section 8.6.2.3 EMAC RGMII Electrical Data/Timing	• Updated/Changed all instances of "at DSP" to "at device"
Section 8.10.1 HDVPSS Electrical Data/Timing	Table 8-42, Timing Requirements for HDVPSS Input: • Deleted NO. 7, $t_{t(CLK)}$, Transition time, VIN[x]A_CLK (10%-90%) • Deleted NO. 7, $t_{t(CLK)}$, Transition time, VIN[x]B_CLK (10%-90%)
Section 8.13.4, DDR2/DDR3 Memory Controller Electrical Data/Timing	Table 8-53, Switching Characteristics Over Recommended Operating Conditions for DDR2/DDR3 Memory Controller: • Updated/Changed NO. 1, $t_{c(DDR\_CLK)}$, Cycle time, DDR[x]_CLK, **DDR2/DDR3 mode** to **DDR2 mode** • Added additional row to NO.1, $t_{c(DDR\_CLK)}$, Cycle time, DDR[x]_CLK: **DDR3 mode**
Section 8.13.4.1 DDR2 Routing Specifications	Section 8.13.4.1.1.1, DDR2 Interface Schematic: • Updated/Changed the sentence from, "... pins by pulling the non-inverted DQS pin..." to **"... DDR[x]_DQS[n] pins to the corresponding..."** • Updated/Changed a sentence from, "... inverted DQS pin..." to "... **$\overline{\text{DDR[x]\_DQS[n]}}$ pins..."** • Added sentence, "The DVDD_DDR[x] and VREFSSTL_DDR[x] power..."
Section 8.13.4.1.2 DDR2 CK and ADDR_CTRL Routing	Table 8-63, CK and ADDR_CTRL Routing Specification: • Updated/Changed the "Series terminator,...the DSP" footnote to "Series terminator,..the processor"
Section 8.13.4.2 DDR3 Routing Specifications	Section 8.13.4.2.4, DDR3 Interface Schematic: • Combined 16-Bit and 32-Bit DDR3 Interface subsections • Deleted repeated figure references • Deleted the sentence, "and the unused DQS.....pulled to ground via 1-kΩ resistors." • Added sentence, "The DVDD_DDR[x] and VREFSSTL_DDR[x]..."

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Section 8.13.4.2.4.1 Compatible JEDEC DDR3 Devices	Table 8-66, Compatible JEDEC DDR3 Devices (Per Interface): • Updated/Changed the max clock rate in footnote, "DDR3 devices with speed...." from "400" MHz to "533" MHz
Section 8.14.3 McASP (McASP[5:0]) Electrical Data/Timing	Table 8-78, Timing Requirements for McASP: • Updated/Changed **McASP1 Only** ACLKR/X ext out, MIN value for NO. 5, $t_{su(AFSRX-ACLKRX)}$, Setup time, MCA[x]_AFSR/X input valid before MCA[X]_ACLKR/X from "4" to **"2"** ns. • Updated/Changed **McASP1 Only** ACLKR/X ext out, MIN value for NO. 7,$t_{su(AXR-ACLKRX)}$, Setup time, MCA[x]_AXR input valid before MCA[X]_ACLKR/X from "4" to **"2"** ns.
Section 8.15 Multichannel Buffered Serial Port (McBSP)	Table 8-80, McBSP Registers: • Updated/Changed McBSP HEX ADDRESS range from "0x4700 0000 - 0x4700 00C0" to **"0x4700 0100 – 0x4700 01C0"** (DDR_REG to STATUS_REG) • Added McBSP registers in HEX ADDRESS range **"0x4700 0000 – 0x4700 004C"** (REVNB to DMATXWAKE_EN)
Section 9.1.2 Device and Development-Support Tool Nomenclature	Figure 9-1, Device Nomenclature: • Added "D = -40°C to 90°C, Industrial Temperature" to the TEMPERATURE RANGE area

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

This data manual revision history highlights the technical changes made to the SPRS648A device-specific data manual to make it an SPRS648B revision.

Scope: Applicable updates to the DM814x DaVinci™ Video DMP — SECURE device family, specifically relating to the TMS320DM8148/47 devices (Silicon Revisions 3.0, 2.1), which are now in the production data (PD) stage of development have been incorporated.

- Updated/Changed Power-Up Sequence
- Updated/Changed Power-Down Sequence
- Low-end OPP combinations no longer supported (CVDD_x < CVDD)
- Added RXACTIVE Function (Bit 18) to PINCTRLx Register Description
- Added Power-On Hours (POH) section
- Added Latch-Up Performance Absolute Maximum Ratings
- DDR2/DDR3 supports up to 533 MHz
- OPP50 is **not** supported
- SmartReflex™ (AVS) is **not** supported
- Deep Sleep Mode is **not** supported
- HDMI HDCP encryption is **not** supported

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Global	• Replaced all instances of "DSP/EDMA MMU" with "**System MMU**" • Deleted all references to OPP50 and Deep Sleep Mode • Deleted the TMS320DM8146 device along with any device-specific information; no longer supported
Section 1 Features	• Updated/Changed description the HD Video Processing Subsystem (HDVPSS) • Updated/Changed the Dual 32-Bit DDR2/DDR3 SDRAM Interfaces sub-bullet from "Supports up to DDR2-800 and DDR3-**800**" to "Supports up to DDR2-800 and DDR3-**1066**"
Section 2.2 Device Characteristics	Table 2-2, Characteristics of the Processor: • Updated/Changed the HD Video Processing Subsystem (HDVPSS) row • Updated/Changed Core Logic (V), OPP100, OPP120 range from "0.95 V – 1.20 V" to "1.10 V – 1.20 V"
Section 2.14.5.2 L4 Slow Peripheral Memory Map	Table 2-9, L4 Slow Peripheral Memory Map: • Updated/Changed 0x4818_8000–0x4818_BFFF Device Name from "SmartReflex0/1 Peripheral and Support Registers" to **"Reserved"** • Updated/Changed 0x4819_0000–0x4819_3FFF Device Name from "SmartReflex2/3 Peripheral and Support Registers" to **"Reserved"**
Section 3.2.8 General-Purpose Input/Outputs (GPIOs)	Table 3-12, GP1 Terminal Functions: • Added "The ENLVCMOS bit in the MLBP_DAT_IO_CTRL register...." to the pin descriptions for pins GP1[10:7] (V2, V1, W2, and W1 respectively).
Section 3.2.26 Reserved Pins	Table 3-49, Reserved Terminal Functions: • Updated/Changed TYPE for Signal No. Y14 (RSV4) and AC8 (RSV5) from "S" to **"I"**

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Section 4 Device Configurations	Section 4.3, Pin Multiplexing Control: • Updated/Changed bit 18 from "RSV" to "RXACTIVE"
	Table 4-11, PINCNTL1 – PINCNTL270 (PINCNTLx) Registers Bit Descriptions: • Updated/Changed the MUXMODE[7:0] Description from "Values other than those ..." to **"A value of zero results ..."** • Updated/Changed bit 18 description to now support RXACTIVE
	Table 4-13, PINCNTLx Registers MUXMODE Functions: • Updated/Changed PINCNTL173 row under 0x20 from "UART2_TXD$^{(M1)}$" to **"UART2_TXD$^{(M0)}$"** • Updated/Changed PINCNTL231 under 0x80 from "GP3[30]$^{(M0)}$" to **"GP3[30]$^{(M1)}$"**
	Section 4.4, Handling Unused Pins: • Added "Unless otherwise noted" to the beginning of, "All supply pins must always ..."
Section 6 Device Operating Conditions	Section 6.1, Absolute Maximum Ratings: • Deleted the "V I/O...(Transient Overshoot/Undershoot)" rows of Input and Output voltage ranges • Added Latch-Up Performance row and Latch-Up footnotes • Updated/Changed ESD-HBM footnote to "Level listed is passing level per ANSI/ESDA/JEDEC J5-001..." • Updated/Changed ESD-CDM footnote to "Level listed is passing level per EIA-JEDEC JESD22-C101E..."
	Section 6.3, Power on Hours (POH): • Added Power-On Hour (POH) section **[New]**
Section 7.2.2.1 Dynamic Voltage Frequency Scaling (DVFS)	Table 7-5, Supported OPP Combinations: • Deleted lower-end OPP combinations supported for ARM, DSP, and HDVICP2
Section 7.2.8.1 Power-Up Sequence	Table 7-6 , Power-Up Sequence Ramping Values: • Added NO. 1 MIN value of "0" ms. • Updated/Changed NO. 1 description to "1.8 V and DVDD_DDR[x] supplies stable..." • Added NO. 13, "CVDD variable supply ramp...." • Updated/Changed Figure 7-1 according to table changes • Deleted 3.3 V Supplies Rising Before 1.8 V Supplies Delta Figure (was Figure 7.2) and associated footnote references • Deleted footnote, "The 3.3 V supplies must be..."
Section 7.2.8.2 Power-Down Sequence	Section 7.2.8.2, Power-Down Sequence: • Added, "Ramping down all supplies at the same time...For proper device..." paragraph
	Table 7-7, Power-Down Sequence Ramping Values: • Updated/Changed "The 1.5-/1.8-V DVDD_DDR[x]..." footnote • Updated/Changed figure reference to Figure 7-3 • Added NO. 14, "CVDD_x variable supplies ramp-down..." • Added associated footnote, "CVDD_x must never exceed CVDD by more than 150mV"
	Figure 7-2, Power-Down Sequence: • Updated/Changed figure according to table changes
	Figure 7-3,1.8 V Supplies Falling Before 3.3 V Supplies Delta: • Added figure **[New]**

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Section 7.4 Clocking	Section 7.4.1.1, Using the Internal Oscillators: Table 7-11, Requirements for Crystal Circuit on the Device Oscillator (DEVOSC): • Added three conditions and the MAX values to the Crystal Frequency Stability PARAMETER
	Table 7-15, Timing Requirements for DEVOSC_MXI/DEV_CLKIN • Added three conditions and the MAX values to the Frequency Stability PARAMETER
	Section 7.4.3, AUD_CLKINx Input Clocks: • Added section **[New]**
	Section 7.4.4, CLKIN32 Input Clock: • Added "/8" to the TIMER1/2/3/4/5/6/7 bullet
	Section 7.4.7, Input/Output Clocks Electrical Data/Timing: • Added Table 7-17, Timing Requirements for AUD_CLKINx **[New]** • Added Figure 7-14, AUD_CLKINx Timing **[New]**
	Section 7.4.8, PLLs: • Deleted PLL Electrical Data/Timing subsection
Section 7.4.9 SYSCLKs	Table 7-26, Maximum SYSCLK Clock Frequencies: • Added footnote, "The maximum frequencies listed..."
Section 7.4.10 Module Clocks	Table 7-27, Maximum Module Clock Frequencies: • Updated/Changed Media Controller **CLOCK SOURCES** from "PLL_MEDIACTL" to "PLL_MEDIACTL/2" • Updated/Changed Media Controller **MAX FREQUENCY OPP100 (MHz)** value from "400" to "200" • Added footnote, "The maximum frequencies listed..."
Section 8.4 EDMA	Section 8.4.1, EDMA Channel Synchronization Events: • Updated/Changed paragraphs
	Section 8.4.2, EDMA Peripheral Register Descriptions: • Added Table 8-5, EDMA Channel Controller (EDMA TPCC) Control Registers • Added Table 8-6, EDMA Transfer Controller (EDMA TPTC) Control Registers
Section 8.5.3 IEEE 1149.1 JTAG	Table 8-8, JTAG ID Register Table: • Added silicon-revision specific information to the VARIANT bit field
Section 8.6.2.3 EMAC RGMII Electrical Data/Timing	• Updated/Changed all instances of "at DSP" to "at device"
Section 8.10.1 HDVPSS Electrical Data/Timing	Table 8-42, Timing Requirements for HDVPSS Input: • Deleted NO. 7, $t_{f(CLK)}$, Transition time, VIN[x]A_CLK (10%-90%) • Deleted NO. 7, $t_{f(CLK)}$, Transition time, VIN[x]B_CLK (10%-90%)
Section 8.13.4, DDR2/DDR3 Memory Controller Electrical Data/Timing	Table 8-53, Switching Characteristics Over Recommended Operating Conditions for DDR2/DDR3 Memory Controller: • Updated/Changed NO. 1, $t_{c(DDR\_CLK)}$, Cycle time, DDR[x]_CLK, **DDR2/DDR3 mode** to **DDR2 mode** • Added additional row to NO.1, $t_{c(DDR\_CLK)}$, Cycle time, DDR[x]_CLK: **DDR3 mode**
Section 8.13.4.1 DDR2 Routing Specifications	Section 8.13.4.1.1.1, DDR2 Interface Schematic: • Updated/Changed the sentence from, "... pins by pulling the non-inverted DQS pin..." to "**... DDR[x]_DQS[n] pins to the corresponding...**" • Updated/Changed a sentence from, "... inverted DQS pin..." to "... **$\overline{\text{DDR[x]\_DQS[n]}}$ pins...**" • Added sentence, "The DVDD_DDR[x] and VREFSSTL_DDR[x] power..."
Section 8.13.4.1.2 DDR2 CK and ADDR_CTRL Routing	Table 8-63, CK and ADDR_CTRL Routing Specification: • Updated/Changed the "Series terminator,...the DSP" footnote to "Series terminator,..the processor"
Section 8.13.4.2 DDR3 Routing Specifications	Section 8.13.4.2.4, DDR3 Interface Schematic: • Combined 16-Bit and 32-Bit DDR3 Interface subsections • Deleted repeated figure references • Deleted the sentence, "and the unused DQS.....pulled to ground via 1-kΩ resistors." • Added sentence, "The DVDD_DDR[x] and VREFSSTL_DDR[x]..."

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Section 8.13.4.2.4.1 Compatible JEDEC DDR3 Devices	Table 8-66, Compatible JEDEC DDR3 Devices (Per Interface): • Updated/Changed the max clock rate in footnote, "DDR3 devices with speed...." from "400" MHz to "533" MHz
Section 8.14.3 McASP (McASP[5:0]) Electrical Data/Timing	Table 8-78, Timing Requirements for McASP: • Updated/Changed **McASP1 Only** ACLKR/X ext out, MIN value for NO. 5, $t_{su(AFSRX-ACLKRX)}$, Setup time, MCA[x]_AFSR/X input valid before MCA[X]_ACLKR/X from "4" to **"2"** ns. • Updated/Changed **McASP1 Only** ACLKR/X ext out, MIN value for NO. 7,$t_{su(AXR-ACLKRX)}$, Setup time, MCA[x]_AXR input valid before MCA[X]_ACLKR/X from "4" to **"2"** ns.
Section 8.15 Multichannel Buffered Serial Port (McBSP)	Table 8-80, McBSP Registers: • Updated/Changed McBSP HEX ADDRESS range from "0x4700 0000 - 0x4700 00C0" to **"0x4700 0100 – 0x4700 01C0"** (DDR_REG to STATUS_REG) • Added McBSP registers in HEX ADDRESS range **"0x4700 0000 – 0x4700 004C"** (REVNB to DMATXWAKE_EN)
Section 9.1.2 Device and Development-Support Tool Nomenclature	• Added Face Detect suffix to the Device Nomenclature • Added "D = -40°C to 90°C, Industrial Temperature" to the TEMPERATURE RANGE area

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

This data manual revision history highlights the technical changes made to the SPRS694A device-specific data manual to make it an SPRS694B revision.

Scope: Applicable updates to the DRA64x/DRA65x Automotive Media Applications Processors device family, specifically relating to the DRA64x/DRA65x devices(all Silicon Revisions 3.0, 2.1, 1.1, and 1.0, which are now in the production data (PD) stage of development have been incorporated.

- Updated/Changed Power-Up Sequence
- Updated/Changed Power-Down Sequence
- Low-end OPP combinations no longer supported (CVDD_x < CVDD)
- Added RXACTIVE Function (Bit 18) to PINCTRLx Register Description
- Added Automotive POH Profile Table to Absolute Maximum Ratings
- Added Latch-Up Performance Absolute Maximum Ratings
- OPP50 is **not** supported
- SmartReflex™ (AVS) is **not** supported
- Deep Sleep Mode is **not** supported
- HDMI HDCP encryption is **not** supported
- Added new DRx655ATS Device

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Global	• Replaced all instances of "DSP/EDMA MMU" with "**System MMU**" • Deleted all references to OPP50 and Deep Sleep Mode • Deleted references to temperature ranges other than automotive (-40°C to 125°C)
Section 1 Features	• Updated/Changed description the HD Video Processing Subsystem (HDVPSS)
Section 2.1 Device Comparison	Table 2-1, DRA64x/DRA65x Device Comparison: • Added DRx655ATS Device
Section 2.2 Device Characteristics	Table 2-2, Characteristics of the Processor: • Updated/Changed the HD Video Processing Subsystem (HDVPSS) row • Updated/Changed Core Logic (V), OPP100, OPP120 range from "0.95 V – 1.20 V" to "1.10 V – 1.20 V"
Section 2.13.6.2 L4 Slow Peripheral Memory Map	Table 2-10, L4 Slow Peripheral Memory Map: • Updated/Changed 0x4818_8000–0x4818_BFFF Device Name from "SmartReflex0/1 Peripheral and Support Registers" to "**Reserved**" • Updated/Changed 0x4819_0000–0x4819_3FFF Device Name from "SmartReflex2/3 Peripheral and Support Registers" to "**Reserved**"
Section 3.2.8 General-Purpose Input/Outputs (GPIOs)	Table 3-12, GP1 Terminal Functions: • Added "The ENLVCMOS bit in the MLBP_DAT_IO_CTRL register...." to the pin descriptions for pins GP1[10:7] (V2, V1, W2, and W1 respectively).
Section 3.2.30 Reserved Pins	Table 3-54, Reserved Terminal Functions: • Updated/Changed TYPE for Signal No. Y14 (RSV4) and AC8 (RSV5) from "S" to "**I**"

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Section 4 Device Configurations	Section 4.3, Pin Multiplexing Control: • Updated/Changed bit 18 from "RSV" to "RXACTIVE"
	Table 4-11, PINCNTL1 – PINCNTL270 (PINCNTLx) Registers Bit Descriptions: • Updated/Changed the MUXMODE[7:0] Description from "Values other than those ..." to **"A value of zero results ..."** • Updated/Changed bit 18 description to now support RXACTIVE
	Table 4-13, PINCNTLx Registers MUXMODE Functions: • Updated/Changed PINCNTL173 row under 0x20 from "UART2_TXD$^{(M1)}$" to **"UART2_TXD$^{(M0)}$"** • Updated/Changed PINCNTL231 under 0x80 from "GP3[30]$^{(M0)}$" to **"GP3[30]$^{(M1)}$"**
	Section 4.4, Handling Unused Pins: • Added "Unless otherwise noted" to the beginning of, "All supply pins must always ..."
Section 6 Device Operating Conditions	Section 6.1, Absolute Maximum Ratings: • Deleted the "V I/O...(Transient Overshoot/Undershoot)" rows of Input and Output voltage ranges • Added Latch-Up Performance row and Latch-Up footnotes • Added Automotive reliability usage footnote (Operating junction temperature range, T_J)
	Section 6.3, Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature: • Changed I_{DDD}1.8-V I/O TYP from TBD to **"170"** mA
Section 7.2.2.1 Dynamic Voltage Frequency Scaling (DVFS)	Table 7-5, Supported OPP Combinations: • Deleted lower-end OPP combinations supported for ARM, DSP, and HDVICP2
Section 7.2.8.1 Power-Up Sequence	Table 7-6 , Power-Up Sequence Ramping Values: • Added NO. 1 MIN value of "0" ms. • Updated/Changed NO. 1 description to "1.8 V and DVDD_DDR[x] supplies stable..." • Added NO. 13, "CVDD variable supply ramp...." • Updated/Changed Figure 7-1 according to table changes • Deleted 3.3 V Supplies Rising Before 1.8 V Supplies Delta Figure (was Figure 7.2) and associated footnote references • Deleted footnote, "The 3.3 V supplies must be..."
Section 7.2.8.2 Power-Down Sequence	Section 7.2.8.2, Power-Down Sequence: • Added, "Ramping down all supplies at the same time...For proper device..." paragraph
	Table 7-7, Power-Down Sequence Ramping Values: • Updated/Changed "The 1.5-/1.8-V DVDD_DDR[x]..." footnote • Updated/Changed figure reference to Figure 7-3 • Added NO. 14, "CVDD_x variable supplies ramp-down..." • Added associated footnote, "CVDD_x must never exceed CVDD by more than 150mV"
	Figure 7-2, Power-Down Sequence: • Updated/Changed figure according to table changes
	Figure 7-3,1.8 V Supplies Falling Before 3.3 V Supplies Delta: • Added figure **[New]**

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Section 7.4 Clocking	Figure 7-6, System Clocking Overview • Added MLB to SYSCLK4 feed
	Section 7.4.1.1, Using the Internal Oscillators: Table 7-11, Requirements for Crystal Circuit on the Device Oscillator (DEVOSC): • Added three conditions and the MAX values to the Crystal Frequency Stability PARAMETER
	Table 7-15, Timing Requirements for DEVOSC_MXI/DEV_CLKIN • Added three conditions and the MAX values to the Frequency Stability PARAMETER
	Section 7.4.3, AUD_CLKINx Input Clocks: • Added section **[New]**
	Section 7.4.4, CLKIN32 Input Clock: • Added "/8" to the TIMER1/2/3/4/5/6/7 bullet
	Section 7.4.7, Input/Output Clocks Electrical Data/Timing: • Added Table 7-17, Timing Requirements for AUD_CLKINx **[New]** • Added Figure 7-14, AUD_CLKINx Timing **[New]**
	Section 7.4.8, PLLs: • Deleted PLL Electrical Data/Timing subsection
Section 7.4.9 SYSCLKs	Table 7-26, Maximum SYSCLK Clock Frequencies: • Added footnote, "The maximum frequencies listed..."
Section 7.4.10 Module Clocks	Table 7-27, Maximum Module Clock Frequencies: • Updated/Changed Media Controller **CLOCK SOURCES** from "PLL_MEDIACTL" to "PLL_MEDIACTL/2" • Updated/Changed Media Controller **MAX FREQUENCY OPP100 (MHz)** value from "400" to "200" • Added MLB row • Added footnote, "The maximum frequencies listed..."
Section 8.5 EDMA	Section 8.5.1, EDMA Channel Synchronization Events: • Updated/Changed paragraphs
	Section 8.5.2, EDMA Peripheral Register Descriptions: • Added Table 8-6, EDMA Channel Controller (EDMA TPCC) Control Registers • Added Table 8-7, EDMA Transfer Controller (EDMA TPTC) Control Registers
Section 8.6.3 IEEE 1149.1 JTAG	Table 8-9, JTAG ID Register Table: • Added silicon-revision specific information to the VARIANT bit field
Section 8.7.2.3 EMAC RGMII Electrical Data/Timing	• Updated/Changed all instances of "at DSP" to "at device"
Section 8.11.1 HDVPSS Electrical Data/Timing	Table 8-43, Timing Requirements for HDVPSS Input: • Deleted NO. 7, $t_{t(CLK)}$, Transition time, VIN[x]A_CLK (10%-90%) • Deleted NO. 7, $t_{t(CLK)}$, Transition time, VIN[x]B_CLK (10%-90%)
Section 8.14.4.1 DDR2 Routing Specifications	Section 8.14.4.1.1.1, DDR2 Interface Schematic: • Updated/Changed the sentence from, "... pins by pulling the non-inverted DQS pin..." to "**... DDR[x]_DQS[n] pins to the corresponding...**" • Updated/Changed a sentence from, "... inverted DQS pin..." to "... **$\overline{\text{DDR[x]\_DQS[n]}}$ pins...**" • Added sentence, "The DVDD_DDR[x] and VREFSSTL_DDR[x] power..."
Section 8.14.4.1.2 DDR2 CK and ADDR_CTRL Routing	Table 8-64, CK and ADDR_CTRL Routing Specification: • Updated/Changed the "Series terminator,...the DSP" footnote to "Series terminator,..the processor"
Section 8.14.4.2 DDR3 Routing Specifications	Section 8.14.4.2.4, DDR3 Interface Schematic: • Combined 16-Bit and 32-Bit DDR3 Interface subsections • Deleted repeated figure references • Deleted the sentence, "and the unused DQS.....pulled to ground via 1-kΩ resistors." • Added sentence, "The DVDD_DDR[x] and VREFSSTL_DDR[x]..."

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Section 8.15.3 McASP (McASP[5:0]) Electrical Data/Timing	Table 8-79, Timing Requirements for McASP: • Updated/Changed **McASP1 Only** ACLKR/X ext out, MIN value for NO. 5, $t_{su(AFSRX-ACLKRX)}$, Setup time, MCA[x]_AFSR/X input valid before MCA[X]_ACLKR/X from "4" to **"2"** ns. • Updated/Changed **McASP1 Only** ACLKR/X ext out, MIN value for NO. 7,$t_{su(AXR-ACLKRX)}$, Setup time, MCA[x]_AXR input valid before MCA[X]_ACLKR/X from "4" to **"2"** ns.
Section 8.16 Multichannel Buffered Serial Port (McBSP)	Table 8-81, McBSP Registers: • Updated/Changed McBSP HEX ADDRESS range from "0x4700 0000 - 0x4700 00C0" to **"0x4700 0100 – 0x4700 01C0"** (DDR_REG to STATUS_REG) • Added McBSP registers in HEX ADDRESS range **"0x4700 0000 – 0x4700 004C"** (REVNB to DMATXWAKE_EN)
Section 9.1.2 Device and Development-Support Tool Nomenclature	• Updated/Changed "TI device nomenclature also includes ..." paragraph
	Figure 9-1, Device Nomenclature: • Deleted the Commercial Temperature and Extended Temperature from the TEMPERATURE RANGE area • Added DRA6555ATS Device

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

This data manual revision history highlights the technical changes made to the SPRS695B device-specific data manual to make it an SPRS695C revision.

Scope: Applicable updates to the AM387x Sitara™ ARM Processor device family, specifically relating to the AM3874/1 devices (Silicon Revisions 3.0, 2.1), which are now in the production data (PD) stage of development have been incorporated.

- Updated/Changed Power-Up Sequence
- Updated/Changed Power-Down Sequence
- Low-end OPP combinations no longer supported (CVDD_x < CVDD)
- Added RXACTIVE Function (Bit 18) to PINCTRLx Register Description
- Added Power-On Hours (POH) section
- Added Latch-Up Performance Absolute Maximum Ratings
- DDR2/DDR3 supports up to 533 MHz
- OPP50 is **not** supported
- SmartReflex™ (AVS) is **not** supported
- Deep Sleep Mode is **not** supported
- HDMI HDCP encryption is **not** supported

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Global	• Replaced all instances of "DSP/EDMA MMU" with "**System MMU**" • Deleted all references to OPP50 and Deep Sleep Mode • Deleted the AM3872 device along with any device-specific information; no longer supported
Section 1 Features	• Updated/Changed description the HD Video Processing Subsystem (HDVPSS) • Updated/Changed the Dual 32-Bit DDR2/DDR3 SDRAM Interfaces sub-bullet from "Supports up to DDR2-800 and DDR3-**800**" to "Supports up to DDR2-800 and DDR3-**1066**"
Section 2.2 Device Characteristics	Table 2-2, Characteristics of the Processor: • Updated/Changed the HD Video Processing Subsystem (HDVPSS) row • Updated/Changed Core Logic (V), OPP100, OPP120 range from "0.95 V – 1.20 V" to "1.10 V – 1.20 V"
Section 2.9.2.2 L4 Slow Peripheral Memory Map	Table 2-5, L4 Slow Peripheral Memory Map: • Updated/Changed 0x4818_8000–0x4818_BFFF Device Name from "SmartReflex0/1 Peripheral and Support Registers" to "**Reserved**"
Section 3.2.7 General-Purpose Input/Outputs (GPIOs)	Table 3-11, GP1 Terminal Functions: • Added "The ENLVCMOS bit in the MLBP_DAT_IO_CTRL register...." to the pin descriptions for pins GP1[10:7] (V2, V1, W2, and W1 respectively).
Section 3.2.25 Reserved Pins	Table 3-48, Reserved Terminal Functions: • Updated/Changed TYPE for Signal No. Y14 (RSV4) and AC8 (RSV5) from "S" to "**I**"

Section 4 Device Configurations	Section 4.3, Pin Multiplexing Control: • Updated/Changed bit 18 from "RSV" to "RXACTIVE"
	Table 4-11, PINCNTL1 – PINCNTL270 (PINCNTLx) Registers Bit Descriptions: • Updated/Changed the MUXMODE[7:0] Description from "Values other than those ..." to **"A value of zero results ..."** • Updated/Changed bit 18 description to now support RXACTIVE
	Table 4-13, PINCNTLx Registers MUXMODE Functions: • Updated/Changed PINCNTL173 row under 0x20 from "UART2_TXD(M1)" to **"UART2_TXD(M0)"** • Updated/Changed PINCNTL231 under 0x80 from "GP3[30](M0)" to **"GP3[30](M1)"**
	Section 4.4, Handling Unused Pins: • Added "Unless otherwise noted" to the beginning of, "All supply pins must always ..."

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Section 6 Device Operating Conditions	Section 6.1, Absolute Maximum Ratings: • Deleted the "V I/O...(Transient Overshoot/Undershoot)" rows of Input and Output voltage ranges • Added Latch-Up Performance row and Latch-Up footnotes • Updated/Changed ESD-HBM footnote to "Level listed is passing level per ANSI/ESDA/JEDEC J5-001..." • Updated/Changed ESD-CDM footnote to "Level listed is passing level per EIA-JEDEC JESD22-C101E..."
	Section 6.3, Power on Hours (POH): • Added Power-On Hour (POH) section **[New]**
Section 7.2.2.1 Dynamic Voltage Frequency Scaling (DVFS)	Table 7-5, Supported OPP Combinations: • Deleted lower-end OPP combinations supported for ARM
Section 7.2.8.1 Power-Up Sequence	Table 7-6 , Power-Up Sequence Ramping Values: • Added NO. 1 MIN value of "0" ms. • Updated/Changed NO. 1 description to "1.8 V and DVDD_DDR[x] supplies stable..." • Added NO. 13, "CVDD variable supply ramp...." • Updated/Changed Figure 7-1 according to table changes • Deleted 3.3 V Supplies Rising Before 1.8 V Supplies Delta Figure (was Figure 7.2) and associated footnote references • Deleted footnote, "The 3.3 V supplies must be..."
Section 7.2.8.2 Power-Down Sequence	Section 7.2.8.2, Power-Down Sequence: • Added, "Ramping down all supplies at the same time...For proper device..." paragraph
	Table 7-7, Power-Down Sequence Ramping Values: • Updated/Changed "The 1.5-/1.8-V DVDD_DDR[x]..." footnote • Updated/Changed figure reference to Figure 7-3 • Added NO. 14, "CVDD_x variable supplies ramp-down..." • Added associated footnote, "CVDD_x must never exceed CVDD by more than 150mV"
	Figure 7-2, Power-Down Sequence: • Updated/Changed figure according to table changes
	Figure 7-3,1.8 V Supplies Falling Before 3.3 V Supplies Delta: • Added figure **[New]**

Section 7.4 Clocking	Section 7.4.1.1, Using the Internal Oscillators: Table 7-11, Requirements for Crystal Circuit on the Device Oscillator (DEVOSC): • Added three conditions and the MAX values to the Crystal Frequency Stability PARAMETER
	Table 7-15, Timing Requirements for DEVOSC_MXI/DEV_CLKIN • Added three conditions and the MAX values to the Frequency Stability PARAMETER
	Section 7.4.3, AUD_CLKINx Input Clocks: • Added section **[New]**
	Section 7.4.4, CLKIN32 Input Clock: • Added "/8" to the TIMER1/2/3/4/5/6/7 bullet
	Section 7.4.7, Input/Output Clocks Electrical Data/Timing: • Added Table 7-17, Timing Requirements for AUD_CLKINx **[New]** • Added Figure 7-14, AUD_CLKINx Timing **[New]**
	Section 7.4.8, PLLs: • Deleted PLL Electrical Data/Timing subsection
Section 7.4.9 SYSCLKs	Table 7-26, Maximum SYSCLK Clock Frequencies: • Added footnote, "The maximum frequencies listed..."

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Section 7.4.10 Module Clocks	Table 7-27, Maximum Module Clock Frequencies: • Updated/Changed Media Controller **CLOCK SOURCES** from "PLL_MEDIACTL" to "PLL_MEDIACTL/2" • Updated/Changed Media Controller **MAX FREQUENCY OPP100 (MHz)** value from "400" to "200" • Added footnote, "The maximum frequencies listed..."
Section 8.4 EDMA	Section 8.4.1, EDMA Channel Synchronization Events: • Updated/Changed paragraphs
	Section 8.4.2, EDMA Peripheral Register Descriptions: • Added Table 8-5, EDMA Channel Controller (EDMA TPCC) Control Registers • Added Table 8-6, EDMA Transfer Controller (EDMA TPTC) Control Registers
Section 8.5.3 IEEE 1149.1 JTAG	Table 8-8, JTAG ID Register Table: • Added silicon-revision specific information to the VARIANT bit field
Section 8.6.2.3 EMAC RGMII Electrical Data/Timing	• Updated/Changed all instances of "at DSP" to "at device"
Section 8.10.1 HDVPSS Electrical Data/Timing	Table 8-42, Timing Requirements for HDVPSS Input: • Deleted NO. 7, $t_{f(CLK)}$, Transition time, VIN[x]A_CLK (10%-90%) • Deleted NO. 7, $t_{f(CLK)}$, Transition time, VIN[x]B_CLK (10%-90%)
Section 8.13.4, DDR2/DDR3 Memory Controller Electrical Data/Timing	Table 8-53, Switching Characteristics Over Recommended Operating Conditions for DDR2/DDR3 Memory Controller: • Updated/Changed NO. 1, $t_{c(DDR\_CLK)}$, Cycle time, DDR[x]_CLK, **DDR2/DDR3 mode** to **DDR2 mode** • Added additional row to NO.1, $t_{c(DDR\_CLK)}$, Cycle time, DDR[x]_CLK: **DDR3 mode**
Section 8.13.4.1 DDR2 Routing Specifications	Section 8.13.4.1.1.1, DDR2 Interface Schematic: • Updated/Changed the sentence from, "... pins by pulling the non-inverted DQS pin..." to **"... DDR[x]_DQS[n] pins to the corresponding..."** • Updated/Changed a sentence from, "... inverted DQS pin..." to "... **$\overline{\text{DDR[x]\_DQS[n]}}$ pins..."** • Added sentence, "The DVDD_DDR[x] and VREFSSTL_DDR[x] power..."
Section 8.13.4.1.2 DDR2 CK and ADDR_CTRL Routing	Table 8-63, CK and ADDR_CTRL Routing Specification: • Updated/Changed the "Series terminator,...the DSP" footnote to "Series terminator,..the processor"
Section 8.13.4.2 DDR3 Routing Specifications	Section 8.13.4.2.4, DDR3 Interface Schematic: • Combined 16-Bit and 32-Bit DDR3 Interface subsections • Deleted repeated figure references • Deleted the sentence, "and the unused DQS.....pulled to ground via 1-kΩ resistors." • Added sentence, "The DVDD_DDR[x] and VREFSSTL_DDR[x]..."
Section 8.13.4.2.4.1 Compatible JEDEC DDR3 Devices	Table 8-66, Compatible JEDEC DDR3 Devices (Per Interface): • Updated/Changed the max clock rate in footnote, "DDR3 devices with speed...." from "400" MHz to "533" MHz
Section 8.14.3 McASP (McASP[5:0]) Electrical Data/Timing	Table 8-78, Timing Requirements for McASP: • Updated/Changed **McASP1 Only** ACLKR/X ext out, MIN value for NO. 5, $t_{su(AFSRX-ACLKRX)}$, Setup time, MCA[x]_AFSR/X input valid before MCA[X]_ACLKR/X from "4" to **"2"** ns. • Updated/Changed **McASP1 Only** ACLKR/X ext out, MIN value for NO. 7,$t_{su(AXR-ACLKRX)}$, Setup time, MCA[x]_AXR input valid before MCA[X]_ACLKR/X from "4" to **"2"** ns.
Section 8.15 Multichannel Buffered Serial Port (McBSP)	Table 8-80, McBSP Registers: • Updated/Changed McBSP HEX ADDRESS range from "0x4700 0000 - 0x4700 00C0" to **"0x4700 0100 – 0x4700 01C0"** (DDR_REG to STATUS_REG) • Added McBSP registers in HEX ADDRESS range **"0x4700 0000 – 0x4700 004C"** (REVNB to DMATXWAKE_EN)
Section 9.1.2 Device and Development-Support Tool Nomenclature	• Updated/Changed "TI device nomenclature also includes ..." paragraph

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

This data manual revision history highlights the technical changes made to the SPRS712A device-specific data manual to make it an SPRS712B revision and also highlights the technical changes made to the SPRS712B device-specific data manual to make it an SPRS712C revision.

Scope: Applicable updates to the DM812x DaVinci™ Video DMP device family, specifically relating to the TMS320DM8127 devices(Silicon Revision 3.0, 2.1), which are now in the production data (PD) stage of development have been incorporated.

- Added Supported OPP Combinations table (**Revision C Change**)
- Updated/Changed Power-Up Sequence
- Updated/Changed Power-Down Sequence
- Added RXACTIVE Function (Bit 18) to PINCTRLx Register Description
- Added Power-On Hours (POH) section
- Added Latch-Up Performance Absolute Maximum Ratings
- DDR2/DDR3 supports up to 533 MHz
- OPP50 is **not** supported
- SmartReflex™ (AVS) is **not** supported
- Deep Sleep Mode is **not** supported
- HDMI HDCP encryption is **not** supported
- Added new Device Comparison table

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Revision B, December 2013 to Revision C, February 2014	
Global	• Document now released to ti.com • Updated/Changed "DM812x" references to "DM8127"
Section 8.2.2.1 Dynamic Voltage Frequency Scaling (DVFS)	• Added Table 8-5, *Supported OPP Combinations*
Revision A, September 2012 to Revision B, December 2013	
Global	• Replaced all instances of "DSP/EDMA MMU" with "**System MMU**" • Deleted all references to OPP50 and Deep Sleep Mode • Updated/Changed the DM812x Davinci...data manual title
Section 1 Features	• Updated/Changed description the HD Video Processing Subsystem (HDVPSS) • Updated/Changed the Dual 32-Bit DDR2/DDR3 SDRAM Interfaces sub-bullet from "Supports up to DDR2-800 and DDR3-**800**" to "Supports up to DDR2-800 and DDR3-**1066**"
Section 3.1 Device Comparison	Table 3-1, DM8127 Device Comparison: • Added Device Comparison Table **[New]**
Section 3.2 Device Characteristics	Table 3-2, Characteristics of the Processor: • Updated/Changed the HD Video Processing Subsystem (HDVPSS) row • Updated/Changed Core Logic (V), OPP100, OPP120 range from "0.95 V – 1.20 V" to "1.10 V – 1.20 V"
Section 3.12.3.2 L4 Slow Peripheral Memory Map	Table 3-6, L4 Slow Peripheral Memory Map: • Updated/Changed 0x4818_8000–0x4818_BFFF Device Name from "SmartReflex0/1 Peripheral and Support Registers" to **"Reserved"** • Updated/Changed 0x4819_0000–0x4819_3FFF Device Name from "SmartReflex2/3 Peripheral and Support Registers" to **"Reserved"**

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Section 4.2.8 General-Purpose Input/Outputs (GPIOs)	Table 4-12, GP1 Terminal Functions: • Added "The ENLVCMOS bit in the MLBP_DAT_IO_CTRL register...." to the pin descriptions for pins GP1[10:7] (V2, V1, W2, and W1 respectively).
Section 4.2.25 Reserved Pins	Table 4-47, Reserved Terminal Functions: • Updated/Changed TYPE for Signal No. Y14 (RSV4) and AC8 (RSV5) from "S" to **"I"**
Section 5 Device Configurations	Section 5.3, Pin Multiplexing Control: • Updated/Changed bit 18 from "RSV" to "RXACTIVE"
	Table 5-11, PINCNTL1 – PINCNTL270 (PINCNTLx) Registers Bit Descriptions: • Updated/Changed the MUXMODE[7:0] Description from "Values other than those ..." to **"A value of zero results ..."** • Updated/Changed bit 18 description to now support RXACTIVE
	Table 5-13, PINCNTLx Registers MUXMODE Functions: • Updated/Changed PINCNTL173 row under 0x20 from "UART2_TXD$^{(M1)}$" to **"UART2_TXD$^{(M0)}$"** • Updated/Changed PINCNTL231 under 0x80 from "GP3[30]$^{(M0)}$" to **"GP3[30]$^{(M1)}$"**
	Section 5.4, Handling Unused Pins: • Added "Unless otherwise noted" to the beginning of, "All supply pins must always ..."
Section 7 Device Operating Conditions	Section 7.1, Absolute Maximum Ratings: • Deleted the "V I/O...(Transient Overshoot/Undershoot)" rows of Input and Output voltage ranges • Added Latch-Up Performance row and Latch-Up footnotes • Updated/Changed ESD-HBM footnote to "Level listed is passing level per ANSI/ESDA/JEDEC J5-001..." • Updated/Changed ESD-CDM footnote to "Level listed is passing level per EIA-JEDEC JESD22-C101E..."
	Section 7.3, Power on Hours (POH): • Added Power-On Hour (POH) section **[New]**
Section 8.2.2.1 Dynamic Voltage Frequency Scaling (DVFS)	Table 8-4, Device Operating Points (OPPs): • Updated/Changed the CYEx0, 120% (1.2 V) Cortex A8 (MHz) speed from "–" to "720" • Updated/Changed the CYEx0, 120% (1.2 V) DSP (MHz) speed from "–" to "600" • Updated/Changed the CYEx2, 166% (1.35 V) DSP (MHz) speed from "–" to "700" • Updated/Changed the CYEx2, 166% (1.35 V) HDVICP2 (MHz) speed from "430" to "410"
Section 8.2.8.1 Power-Up Sequence	Table 8-6 , Power-Up Sequence Ramping Values: • Added NO. 1 MIN value of "0" ms. • Updated/Changed NO. 1 description to "1.8 V and DVDD_DDR[x] supplies stable..." • Added NO. 13, "CVDD variable supply ramp...." • Updated/Changed Figure 8-1 according to table changes • Deleted 3.3 V Supplies Rising Before 1.8 V Supplies Delta Figure (was Figure 7.2) and associated footnote references • Deleted footnote, "The 3.3 V supplies must be..."
Section 8.2.8.2 Power-Down Sequence	Section 8.2.8.2, Power-Down Sequence: • Added, "Ramping down all supplies at the same time...For proper device..." paragraph
	Table 8-7, Power-Down Sequence Ramping Values: • Updated/Changed "The 1.5-/1.8-V DVDD_DDR[x]..." footnote • Updated/Changed figure reference to Figure 8-3 • Added NO. 14, "CVDD_x variable supplies ramp-down..." • Added associated footnote, "CVDD_x must never exceed CVDD by more than 150mV"
	Figure 8-2, Power-Down Sequence: • Updated/Changed figure according to table changes
	Figure 8-3,1.8 V Supplies Falling Before 3.3 V Supplies Delta: • Added figure **[New]**

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Section 8.4 Clocking	Section 8.4.1.1, Using the Internal Oscillators: Table 8-11, Requirements for Crystal Circuit on the Device Oscillator (DEVOSC): • Added three conditions and the MAX values to the Crystal Frequency Stability PARAMETER
	Table 8-15, Timing Requirements for DEVOSC_MXI/DEV_CLKIN • Added three conditions and the MAX values to the Frequency Stability PARAMETER
	Section 8.4.3, AUD_CLKINx Input Clocks: • Added section **[New]**
	Section 8.4.4, CLKIN32 Input Clock: • Added "/8" to the TIMER1/2/3/4/5/6/7 bullet
	Section 8.4.7, Input/Output Clocks Electrical Data/Timing: • Added Table 8-17, Timing Requirements for AUD_CLKINx **[New]** • Added Figure 8-14, AUD_CLKINx Timing **[New]**
	Section 8.4.8, PLLs: • Deleted PLL Electrical Data/Timing subsection
Section 8.4.9 SYSCLKs	Table 8-26, Maximum SYSCLK Clock Frequencies: • Added footnote, "The maximum frequencies listed..."
Section 8.4.10 Module Clocks	Table 8-27, Maximum Module Clock Frequencies: • Updated/Changed Media Controller **CLOCK SOURCES** from "PLL_MEDIACTL" to "PLL_MEDIACTL/2" • Updated/Changed Media Controller **MAX FREQUENCY OPP100 (MHz)** value from "400" to "200" • Added footnote, "The maximum frequencies listed..."
Section 9.4 EDMA	Section 9.4.1, EDMA Channel Synchronization Events: • Updated/Changed paragraphs
	Section 9.4.2, EDMA Peripheral Register Descriptions: • Added Table 9-5, EDMA Channel Controller (EDMA TPCC) Control Registers • Added Table 9-6, EDMA Transfer Controller (EDMA TPTC) Control Registers
Section 9.5.3 IEEE 1149.1 JTAG	Table 9-8, JTAG ID Register Table: • Added silicon-revision specific information to the VARIANT bit field
Section 9.6.2.3 EMAC RGMII Electrical Data/Timing	• Updated/Changed all instances of "at DSP" to "at device"
Section 9.10.1 HDVPSS Electrical Data/Timing	Table 9-42, Timing Requirements for HDVPSS Input: • Deleted NO. 7, $t_{t(CLK)}$, Transition time, VIN[x]A_CLK (10%-90%) • Deleted NO. 7, $t_{t(CLK)}$, Transition time, VIN[x]B_CLK (10%-90%)
Section 9.13.4, DDR2/DDR3 Memory Controller Electrical Data/Timing	Table 9-53, Switching Characteristics Over Recommended Operating Conditions for DDR2/DDR3 Memory Controller: • Updated/Changed NO. 1, $t_{c(DDR\_CLK)}$, Cycle time, DDR[x]_CLK, **DDR2/DDR3 mode** to **DDR2 mode** • Added additional row to NO.1, $t_{c(DDR\_CLK)}$, Cycle time, DDR[x]_CLK: **DDR3 mode**
Section 9.13.4.1 DDR2 Routing Specifications	Section 9.13.4.1.1.1, DDR2 Interface Schematic: • Updated/Changed the sentence from, "... pins by pulling the non-inverted DQS pin..." to "**... DDR[x]_DQS[n] pins to the corresponding...**" • Updated/Changed a sentence from, "... inverted DQS pin..." to "... **$\overline{\text{DDR[x]\_DQS[n]}}$ pins...**" • Added sentence, "The DVDD_DDR[x] and VREFSSTL_DDR[x] power..."
Section 9.13.4.1.2 DDR2 CK and ADDR_CTRL Routing	Table 9-63, CK and ADDR_CTRL Routing Specification: • Updated/Changed the "Series terminator,...the DSP" footnote to "Series terminator,..the processor"
Section 9.13.4.2 DDR3 Routing Specifications	Section 9.13.4.2.4, DDR3 Interface Schematic: • Combined 16-Bit and 32-Bit DDR3 Interface subsections • Deleted repeated figure references • Deleted the sentence, "and the unused DQS.....pulled to ground via 1-kΩ resistors." • Added sentence, "The DVDD_DDR[x] and VREFSSTL_DDR[x]..."

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Section 9.13.4.2.4.1 Compatible JEDEC DDR3 Devices	Table 9-66, Compatible JEDEC DDR3 Devices (Per Interface): • Updated/Changed the max clock rate in footnote, "DDR3 devices with speed...." from "400" MHz to "533" MHz
Section 9.14.3 McASP (McASP[5:0]) Electrical Data/Timing	Table 9-78, Timing Requirements for McASP: • Updated/Changed **McASP1 Only** ACLKR/X ext out, MIN value for NO. 5, $t_{su(AFSRX-ACLKRX)}$, Setup time, MCA[x]_AFSR/X input valid before MCA[X]_ACLKR/X from "4" to **"2"** ns. • Updated/Changed **McASP1 Only** ACLKR/X ext out, MIN value for NO. 7,$t_{su(AXR-ACLKRX)}$, Setup time, MCA[x]_AXR input valid before MCA[X]_ACLKR/X from "4" to **"2"** ns.
Section 9.15 Multichannel Buffered Serial Port (McBSP)	Table 9-80, McBSP Registers: • Updated/Changed McBSP HEX ADDRESS range from "0x4700 0000 - 0x4700 00C0" to **"0x4700 0100 – 0x4700 01C0"** (DDR_REG to STATUS_REG) • Added McBSP registers in HEX ADDRESS range **"0x4700 0000 – 0x4700 004C"** (REVNB to DMATXWAKE_EN)
Section 10.1.2 Device and Development-Support Tool Nomenclature	Figure 10-1, Device Nomenclature: • Deleted DM8128 Device

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Global	• Replaced all instances of "DSP/EDMA MMU" with System MMU • Deleted all references to OPP50, SmartReflex, and Deep Sleep Mode • Updated/Changed all instances of "Microprocessors" to "Processors" • Updated/Changed all instances of "MPU" to "Core"
Section 1.1 Features	• Updated/Changed description for HD Video Processing Subsystem (HDVPSS)
Section 2.2 Device Characteristics	Table 2-2, Characteristics of the Processor: • Updated/Changed the HD Video Processing Subsystem (HDVPSS) row • Updated/Changed Core Logic (V), OPP100, OPP120 range from "0.95 V – 1.20 V" to "1.10 V – 1.20 V" • Added "Flip Chip Ball Grip Array (FCBGA)" to the Package 23 x 23 mm HARDWARE FEATURES column
Section 4 Device Configurations	Table 4-1, PINCNTLx Registers MUXMODE Functions: • Updated/Changed PINCNTL173 row under 0x20 from "UART2_TXD$^{(M1)}$" to **"UART2_TXD$^{(M0)}$"** • Updated/Changed PINCNTL231 under 0x80 from "GP3[30]$^{(M0)}$" to **"GP3[30]$^{(M1)}$"**
Section 5 Device Operating Conditions	Section 5.1, Absolute Maximum Ratings: • Updated/Changed ESD-HBM footnote to "Level listed is passing level per ANSI/ESDA/JEDEC J5-001..." • Updated/Changed ESD-CDM footnote to "Level listed is passing level per EIA-JEDEC JESD22-C101E..." • Added Automotive reliability usage footnote (Operating junction temperature range, T_J)
Section 7.1.2 Device and Development-Support Tool Nomenclature	Figure 7-1, Device Nomenclature: • Added "C = Revision 3.0" to SILICON REVISION • Changed "X" to null "(...)" in part number example
	Figure 7-2, Example, Device Revision Codes for TDA1MSV (CYE Package): • Updated figure to show Silicon Revision 3.0 ("C") example

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

This data manual revision history highlights the technical changes made to the SPRS702 device-specific data manual addendum to make it an SPRS702A revision.

Scope: Applicable updates to the TDA1Mx Automotive Vision Applications Processors device family, specifically relating to the TDA1MED and TDA1MED+ devices (Silicon Revision 3.0), which are now in the production data (PD) stage of development have been incorporated.

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Global	• Updated/Changed all instances of "MPU" to "Core" • Added updates for Global Authoring for Consistency and Translation (for example, no latin abbreviations like e.g. or i.e., removal of "(s)", and so forth)
Section 1.1 Features	• Updated/Changed description for HD Video Processing Subsystem (HDVPSS)
Section 2.1 Device Comparison	Table 2-1, TDA1MSA/SV/ED Device Comparison: • Added SA/SV/ED and SA+/SV+/ED+/ device-specific information to the "Operating Frequency" DSP row • Deleted associated footnote • Split DDR2/DDR3 row into DDR[0] and DDR[1] sub rows to include max speed values
Section 3 Pin Multiplexing Control Differences	Table 3-1, TDA1MED PINCNTLx Registers MUXMODE Functions: • Updated/Changed PINCNTL231 under 0x80 from "GP3[30](M0)" to "GP3[30](M1)"

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

This data manual revision history highlights the technical changes made to the SPRS862 device-specific data manual addendum to make it an SPRS862A revision.

Scope: Applicable updates to the TDA1Mx Automotive Vision Applications Processors device family, specifically relating to the TDA1MED++ devices (Silicon Revision 3.0), which are now in the production data (PD) stage of development have been incorporated.

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Global	• Updated/Changed all instances of "MPU" to "Core" • Added updates for Global Authoring for Consistency and Translation (for example, no latin abbreviations like e.g. or i.e., removal of "(s)", and so forth)
Section 1.1 Features	• Updated/Changed description for HD Video Processing Subsystem (HDVPSS) • Updated/Changed the DDR2/DDR3 SDRAM from " up to DDR2-667 and DDR3-667" to "up to DDR2-800 and DDR3-800"
Section 2.1 Device Comparison	Table 2-1, TDA1MSA/SV/ED Device Comparison: • Added SA/SV/ED and SA+/SV+/ED+/ED++ device-specific information to the "Operating Frequency" DSP row • Deleted associated footnote • Split DDR2/DDR3 row into DDR[0] and DDR[1] sub rows to include max speed values
Section 3 Pin Multiplexing Control Differences	Table 3-1, TDA1MED++ PINCNTLx Registers MUXMODE Functions: • Updated/Changed PINCNTL231 under 0x80 from "GP3[30](M0)" to "GP3[30](M1)"
Section 7 Device and Documentation Support	• Added Nomenclature (Figure 7-1) and Die (Figure 7-2) graphics

These changes may be reviewed in the device datasheets:

- For non-NDA Data Manuals: www.ti.com
- For NDA Data Manuals: In device CDDS folder (contact your TI Representative for details)

Reason for Change:

Electrical specification performance changes as indicated above.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

None.

Changes to product identification resulting from this PCN:

None.

Product Affected:

AM3874BCYE100	TDA1MEDBCYEQ7Q1	TMS320DM8127BCYED1	TMS320DM8148CCYE1
AM3874BCYE80	TDA1MEDCCYEQ5Q1	TMS320DM8127BCYED2	TMS320DM8148CCYE2
DM8147BCIS0	TDA1MSACCYEQ4Q1	TMS320DM8127BCYED3	TMS320DM8148CCYE2F
DM8148CR2CYE2	TDA1MSVBCYEQ4Q1	TMS320DM8147BCYE0	TMS320DM8148CCYEA0
DRA644BICYEQ1	TDA1MSVBCYEQ5Q1	TMS320DM8147BCYE1	TMS320DM8148SCYE0
DRA646BICYEQ1	TDA1MSVCCYEQ4Q1	TMS320DM8147BCYE2	TMS320DM8148SCYE1
DRA655AVWBICYERQ1	TDA1MSVCCYEQ5Q1	TMS320DM8147SCYE0	TMS320DM8148SCYE2
DVITDM8148CCYE1	TMS320DM8127BCYE0	TMS320DM8147SCYE1	TMS320DM8148SCYEA0
HPSDM8148CCYE2	TMS320DM8127BCYE1	TMS320DM8147SCYE2	TMX320DM8148CCYE2
HPXDM8148CCYE2	TMS320DM8127BCYE2	TMS320DM8148BCYE0	ZDM8147L3MOBCYE1
MTDM8148CCYE2	TMS320DM8127BCYE3	TMS320DM8148BCYE1	
TDA1MDRCCYEA0	TMS320DM8127BCYE3L	TMS320DM8148BCYE2	
TDA1MEDBCYEQ5Q1	TMS320DM8127BCYED0	TMS320DM8148CCYE0	

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