miClockManagement Clock Fanout Buffer Product Preview

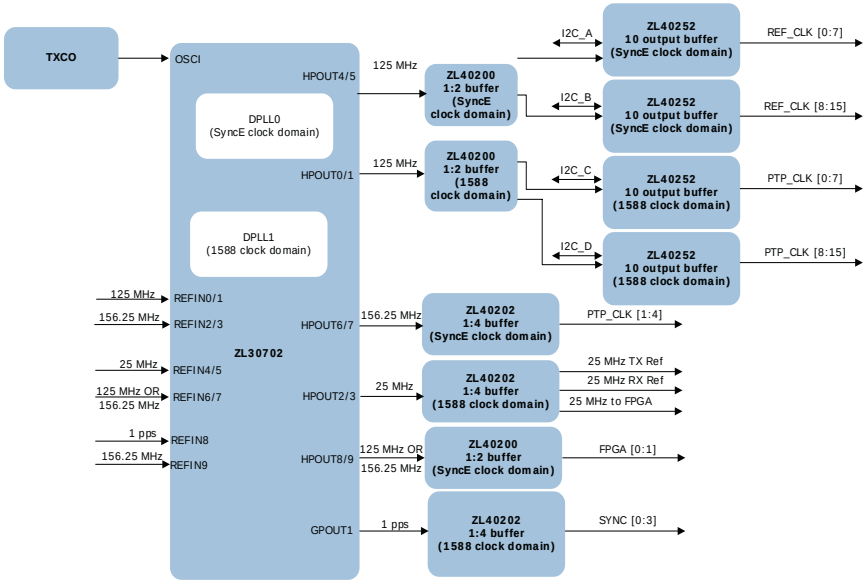
Microsemi's portfolio of miClockBuffer™ and miSmartBuffer™ clock fanout buffers are synergistic with Microsemi's industry-leading timing portfolio—when combined with miClockSynth™ synthesizers, they can create a simplified, more reliable, and low-cost complete clock tree that replaces many on-board multipliers, synthesizers, and oscillators.

Microsemi's miClockBuffer ZL402xx family of buffers offers six fanout combinations with LVPECL or LVDS output types and internal and external terminations. The miClockBuffer and miSmartBuffer ZL4023x and ZL4024x family of devices are offered in a variety of input and output configurations including LVPECL, LVDS, HCSL, and LVCMOS. The portolio also includes the miSmartBuffer ZL4025x family of devices, differentiated from traditional fanout buffers by compelling features including dividers and configurable outputs.

Applications

- Clock signal fanout, format conversion, frequency division, and skew adjustment in a wide variety of equipment types, including processors, NPUs, FPGAs, 10G CDRs, high-speed ADCs and DACs, PCIe interface devices, Ethernet switches, and PHYs
- Clock trees for optical, OTN, SONET, SDH, WDM, storage, networking, and broadcast video applications

IEEE 1588/SyncE Clock Tree



Benefits

- Reduces BOM cost and board space—enables designers to create larger clock trees or simplify small clock trees, leading to significant cost savings
- Increased design efficiency—highly configurable outputs, multiple pin-compatible variants, and multiple input and output configurations (up to eight custom configurations can be created with the miSmartBuffer 25x family)

miClockBuffer ZL402xx Family

- Clock rates up to 750 MHz
- LVPECL, LVDS, CML, HCSL or LVCMOS inputs with devices with internal or external input termination available
- LVPECL or LVDS outputs
- Six fanout combinations—1:2, 1:4, 1:6, 1:8, 2:6, and 2:8
- Ultra-low additive jitter (as low as 39 fs RMS)

miClockBuffer ZL4023x/ZL4024x Family

- Up to three inputs/crystal input/inverted mesa/high-speed crystal
- Up to 10 LVPECL/LVDS/HCSL or 10 LVCMOS outputs
- Low skew and ultra-low additive jitter, as low as 25 fs RMS (12 kHz to 20 mHz)
- miSmartbuffer ZL4023x/ZL4024x family also adds a serial port interface and integer dividers on the LVCMOS outputs

miSmartBuffer ZL4025x Family

- 4 flexible input clocks allow interfacing to a wide variety of devices—crystal/XO, two differential/CMOS, and one single-ended/CMOS
- Frequency conversion—each output has independent divider
- Improve alignment and skew with per-output skew adjustment, per-output enable/disable and glitchless start/stop
- Easily interface—each output configurable as LVDS, LVPECL, HCSL, 2x CMOS, or HSTL

Availability and Support

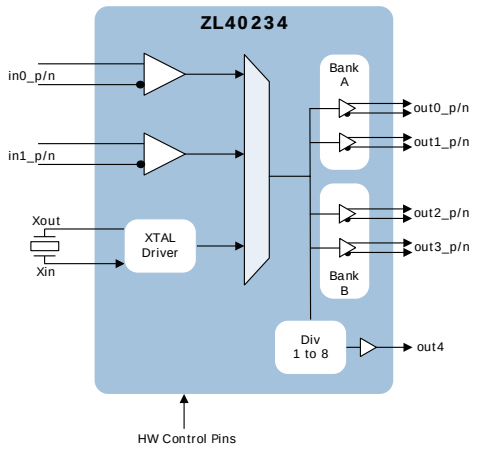
Microsemi miClockManagement products are in volume production. To learn more about Microsemi's clock fanout buffers, visit https://www.microsemi.com/products/timing-and-synchronization/clock-fan-out-buffers.

Full information, including complete datasheets and design manuals, is available to registered MyMicrosemi customers.

miClockManagement Clock Fanout Buffer Product Preview

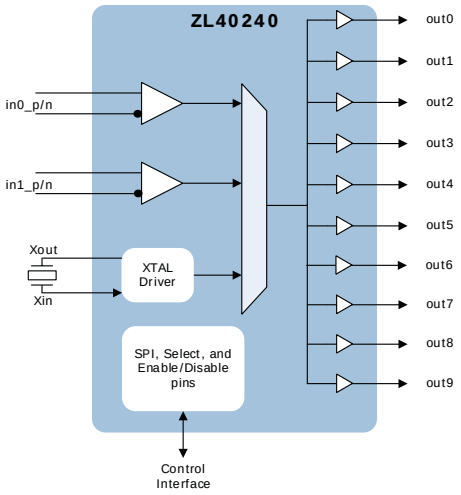
miClockBuffer: ZL40234

- 3-to-1 input multiplexer
- Four differential LVPECL/LVDS/HCSL outputs
- One LVCMOS output
- Ultra-low additive jitter: 25 fs (12 kHz to 20 MHz)
- Supports clock frequencies from 0 GHz to 1.6 GHz
- Supports 2.5 V or 3.3 V power supplies
- Embedded low drop out (LDO) voltage regulator
- Maximum output-to-output skew of 50 ps
- Device-controlled hardware control pins



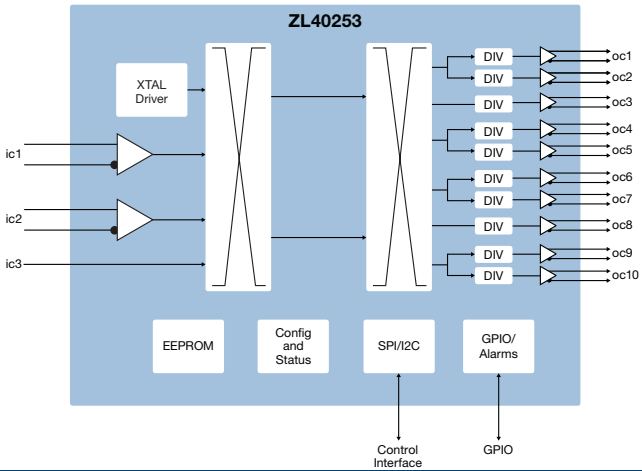
miSmartBuffer: ZL40240

- 3-to-1 input multiplexer
- Ten 1.5 V/1.8 V/2.5 V/3.3 V LVCMOS outputs
- Supports frequencies from 0 MHz to 250 MHz
- Ultra-low additive jitter: 25 fs (12k Hz to 20 MHz)
- Ultra-low noise floor of –170 dBc/Hz
- Supports crystals from 8 MHz to 160 MHz
- Supports 2.5 V or 3.3 V power supplies
- Maximum output-to-output skew of 30 ps
- Input to output delay of 2 ns (typical)
- Device controlled through SPI or hardware control pins



miSmartBuffer: ZL40253

- Four flexible input clocks
- Precise output alignment circuitry controlled by GPIO pin or register bit with per-output skew adjustment
- Per-output enable/disable and glitchless start/stop (stop high or low)
- 10 output clocks, each with an internal divider configurable as LVDS, LVPECL, HCSL, 2x CMOS, or HSTL
- Six flexible power supply banks for 1.5 V/1.8 V/2.5 V/3.3 V
- Create factory-preprogrammed devices with miClockDesigner™ web tool



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