BURR-BROWN®

DAC7612

Dual, 12-Bit Serial Input DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW POWER: 3.7mW
- FAST SETTLING: 7μs to 1 LSB
- 1mV LSB WITH 4.095V FULL-SCALE RANGE
- COMPLETE WITH REFERENCE
- 12-BIT LINEARITY AND MONOTONICITY OVER INDUSTRIAL TEMP RANGE
- 3-WIRE INTERFACE: Up to 20MHz Clock
- SMALL PACKAGE: 8-Lead SOIC

APPLICATIONS

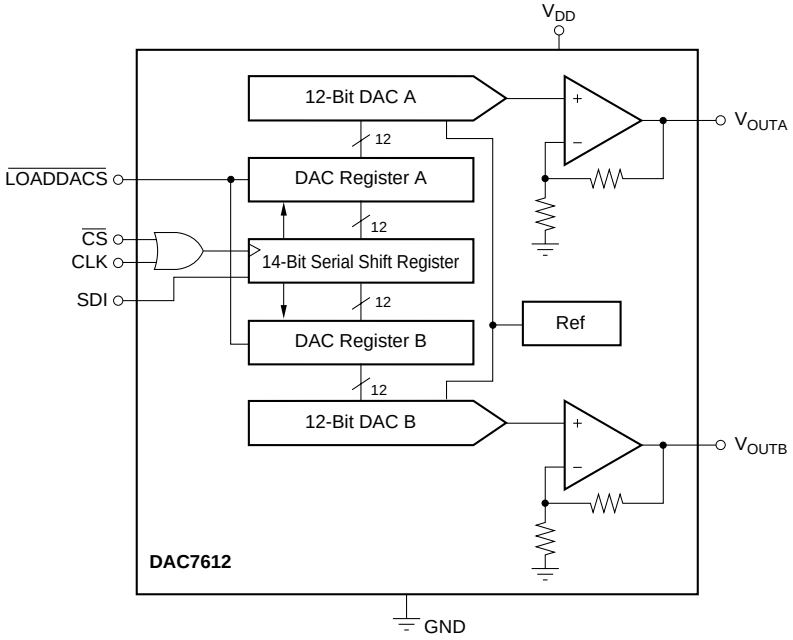
- PROCESS CONTROL
- DATA ACQUISITION SYSTEMS
- CLOSED-LOOP SERVO-CONTROL
- PC PERIPHERALS
- PORTABLE INSTRUMENTATION

DESCRIPTION

The DAC7612 is a dual, 12-bit digital-to-analog converter (DAC) with guaranteed 12-bit monotonicity performance over the industrial temperature range. It requires a single +5V supply and contains an input shift register, latch, 2.435V reference, a dual DAC, and high speed rail-to-rail output amplifiers. For a full-scale step, each output will settle to 1 LSB within 7μs while only consuming 3.7mW.

The synchronous serial interface is compatible with a wide variety of DSPs and microcontrollers. Clock (CLK), Serial Data In (SDI), Chip Select ($\overline{CS}$) and Load DACs ($\overline{LOADDACS}$) comprise the serial interface.

The DAC7612 is available in an 8-lead SOIC package and is fully specified over the industrial temperature range of –40°C to +85°C.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1501A
Printed in U.S.A. June, 1999
SBAS106

SPECIFICATIONS

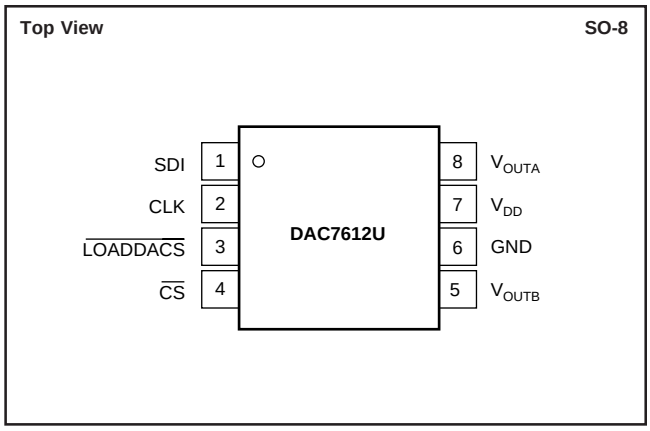
At T_A = –40°C to +85°C, and V_{DD} = +5V, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7612U			DAC7612UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION		12			*			Bits
ACCURACY								
Relative Accuracy[1]		–2	±1/2	+2	–1	±1/4	+1	LSB
Differential Nonlinearity	Guaranteed Monotonic	–1	±1/2	+1	–1	±1/4	+1	LSB
Zero-Scale Error	Code 000_H	–1	+1	+3	*	*	*	LSB
Zero Scale Match	Code 000_H		1/2			1/2	2	LSB
Full-Scale Voltage	Code FFF_H	4.079	4.095	4.111	4.087	4.095	4.103	V
Full-Scale Match	Code FFF_H		1/2			1/2	2	LSB
ANALOG OUTPUT								
Output Current	Code 800_H	±5	±7		*	*		mA
Load Regulation	$R_{LOAD} \geq 402\Omega$, Code 800_H		1	3		*	*	LSB
Capacitive Load	No Oscillation		500			*		pF
Short-Circuit Current			±15			*		mA
Short-Circuit Duration	GND or V_{DD}		Indefinite			*		
DIGITAL INPUT								
Data Format			Serial			*		
Data Coding			Straight Binary			*		
Logic Family			CMOS			*		
Logic Levels								
V_{IH}		0.7 • V_{DD}			*			V
V_{IL}				0.3 • V_{DD}			*	V
I_{IH}				±10			*	µA
I_{IL}				±10			*	µA
DYNAMIC PERFORMANCE								
Settling Time[2] (t_S)	To ±1 LSB of Final Value		7			*		µs
DAC Glitch			2.5			*		nV-s
Digital Feedthrough			0.5			*		nV-s
POWER SUPPLY								
V_{DD}		+4.75	+5.0	+5.25	*	*	*	V
I_{DD}	V_{IH} = 5V, V_{IL} = 0V, No Load, at Code 000_H		0.75	1.5		*	*	mA
Power Dissipation	V_{IH} = 5V, V_{IL} = 0V, No Load		3.5	7.5		*	*	mW
Power Supply Sensitivity	ΔV_{DD} = ±5%		0.0025	0.002		*	*	%/%
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Same specification as for DAC7612U.

NOTES: (1) This term is sometimes referred to as Linearity Error or Integral Nonlinearity (INL). (2) Specification does not apply to negative-going transitions where the final output voltage will be within 3 LSBs of ground. In this region, settling time may be double the value indicated.

PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	LABEL	DESCRIPTION
1	SDI	Serial Data Input. Data is clocked into the internal serial register on the rising edge of CLK.
2	CLK	Synchronous Clock for the Serial Data Input.
3	$\overline{\text{LOADDACS}}$	Loads the internal DAC registers. All DAC registers are transparent latches and are transparent when $\overline{\text{LOADDACS}}$ is LOW (regardless of the state of $\overline{\text{CS}}$ or CLK).
4	$\overline{\text{CS}}$	Chip Select. Active LOW.
5	V_{OUTB}	DAC B Output Voltage
6	GND	Ground
7	V_{DD}	Positive Power Supply
8	V_{OUTA}	DAC A Output Voltage

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to GND	–0.3V to 6V
Digital Inputs to GND	–0.3V to V_{DD} + 0.3V
V_{OUT} to GND	–0.3V to V_{DD} + 0.3V
Power Dissipation	325mW
Thermal Resistance, θ_{JA}	150°C/W
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

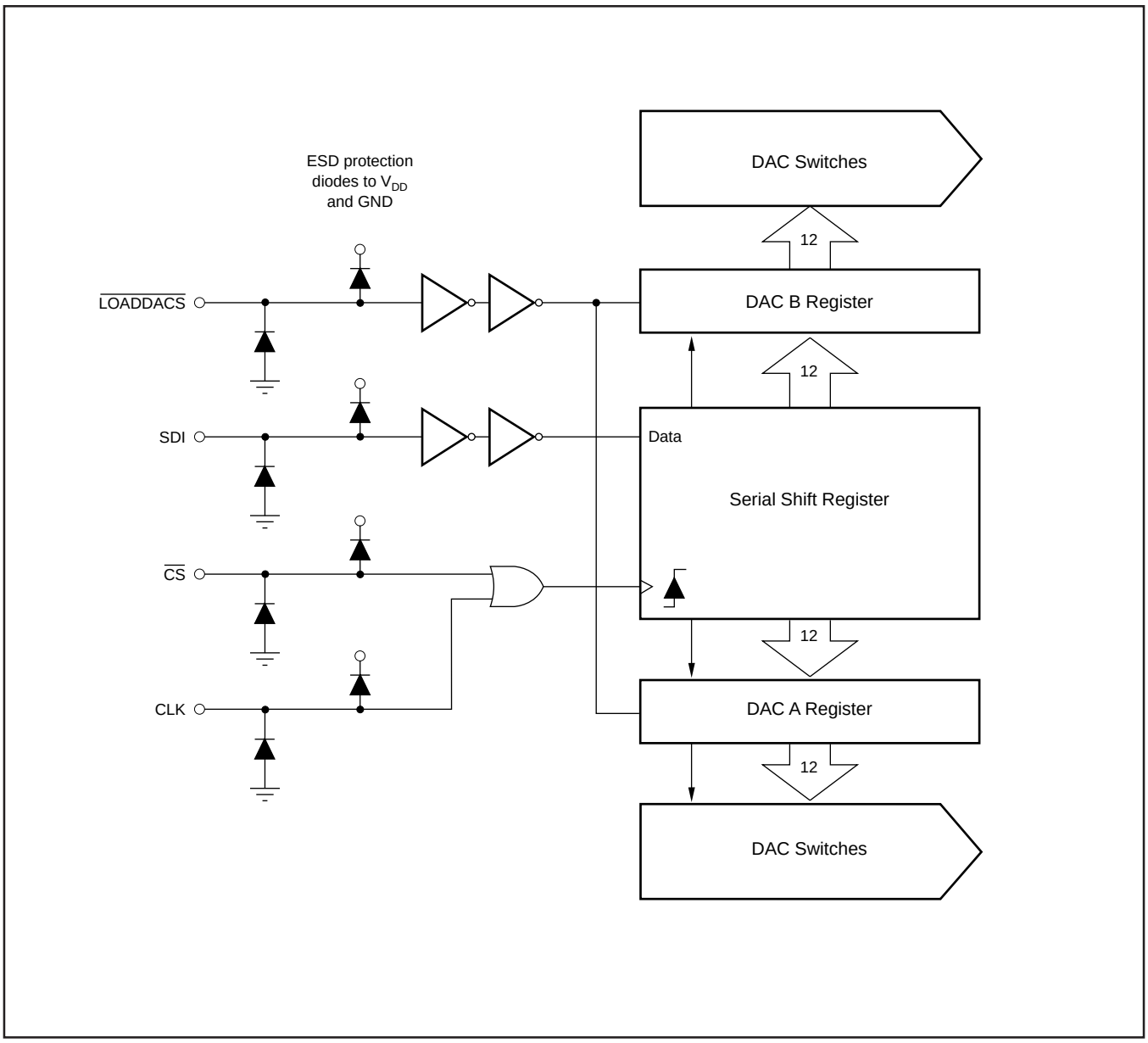
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

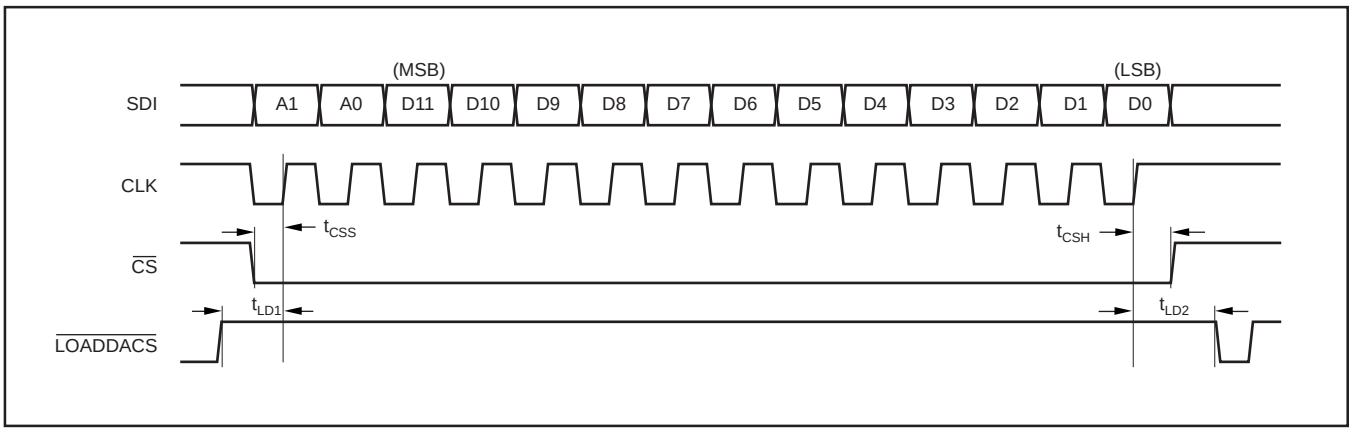
PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE	PACKAGE DRAWING NUMBER[1]	ORDERING NUMBER[2]	TRANSPORT MEDIA
DAC7612U	±2	±1	–40°C to +85°C	SO-8	182	DAC7612U	Rails
"	"	"	"	"	"	DAC7612U/2K5	Tape and Reel
DAC7612UB	±1	±1	–40°C to +85°C	SO-8	182	DAC7612UB	Rails
"	"	"	"	"	"	DAC7612UB/2K5	Tape and Reel

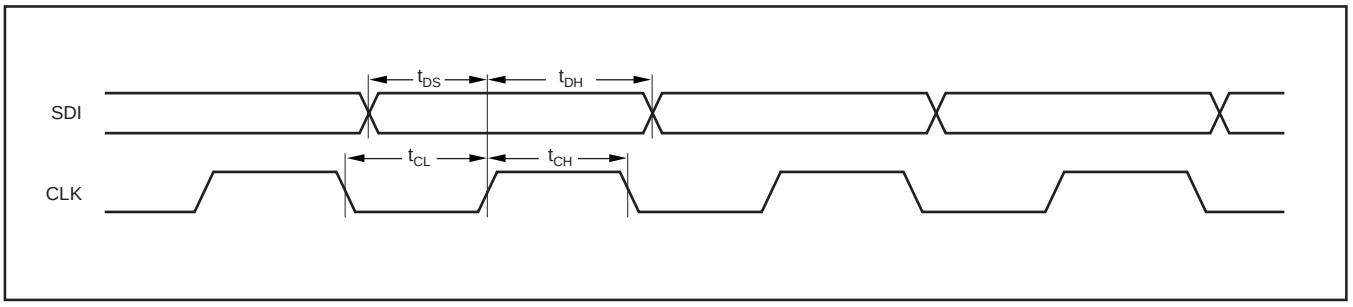
NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "DAC7612U/2K5" will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

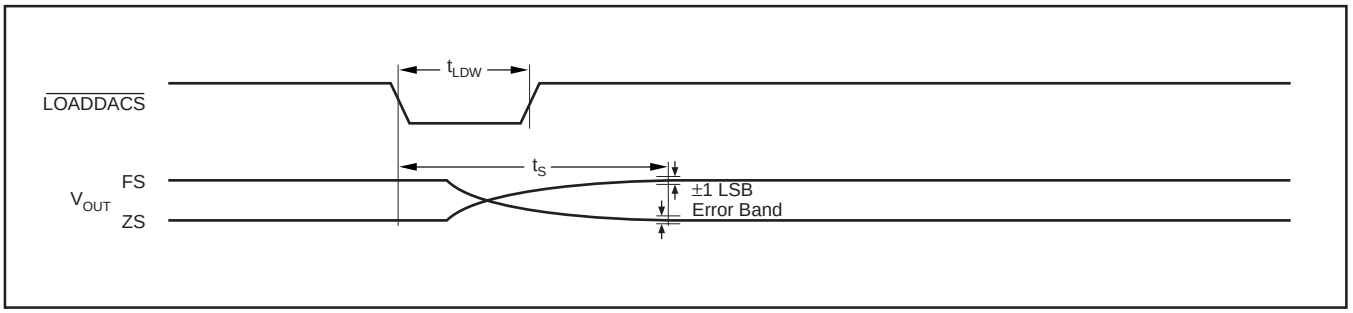
EQUIVALENT INPUT LOGIC



TIMING DIAGRAMS







LOGIC TRUTH TABLE

A1	A0	CLK	$\overline{CS}$	$\overline{LOADDACS}$	SERIAL SHIFT REGISTER	DAC REGISTER A	DAC REGISTER B
X	X	X	H	H	No Change	No Change	No Change
X	X	↑	L	H	Shifts One Bit	No Change	No Change
L	X	X	H(1)	L	No Change	Loads Serial Data Word	Loads Serial Data Word
H	L	X	H	L	No Change	Loads Serial Data Word	No Change
H	H	X	H	L	No Change	No Change	Loads Serial Data Word

↑ Positive Logic Transition; X = Don't Care.

NOTE: (1) A HIGH value is suggested in order to avoid to "false clock" from advancing the shift register and changing the DAC voltage.

DATA INPUT TABLE

B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13
A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

TIMING SPECIFICATIONS

T_A = –40°C to +85°C and V_{DD} = +5V.

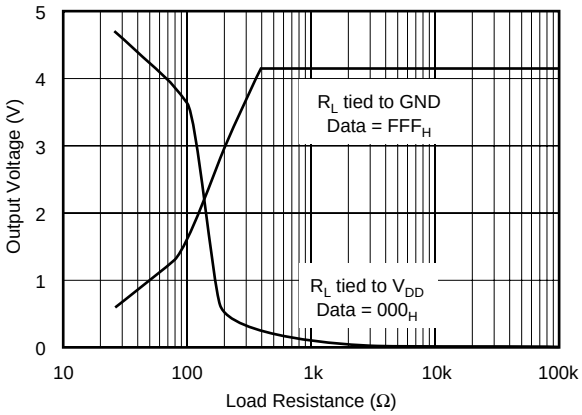
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CH}	Clock Width HIGH	30			ns
t_{CL}	Clock Width LOW	30			ns
t_{LDW}	Load Pulse Width	20			ns
t_{DS}	Data Setup	15			ns
t_{DH}	Data Hold	15			ns
t_{LD1}	Load Setup	15			ns
t_{LD2}	Load Hold	10			ns
t_{CSS}	Select	30			ns
t_{CSH}	Deselect	20			ns

NOTE: All input control signals are specified with $t_R = t_F$ = 5ns (10% to 90% of +5V) and timed from a voltage level of 2.5V. These parameters are guaranteed by design and are not subject to production testing.

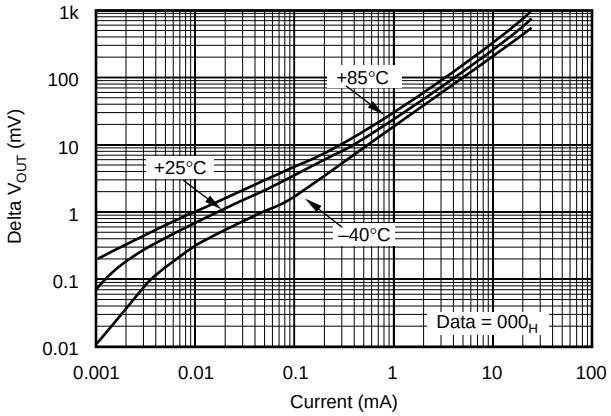
TYPICAL PERFORMANCE CURVES

At T_A = +25°, and V_{DD} = 5V, unless otherwise specified.

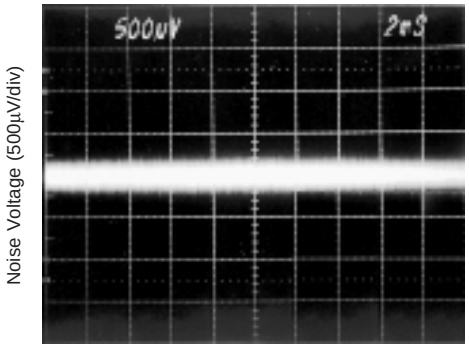
OUTPUT SWING vs LOAD



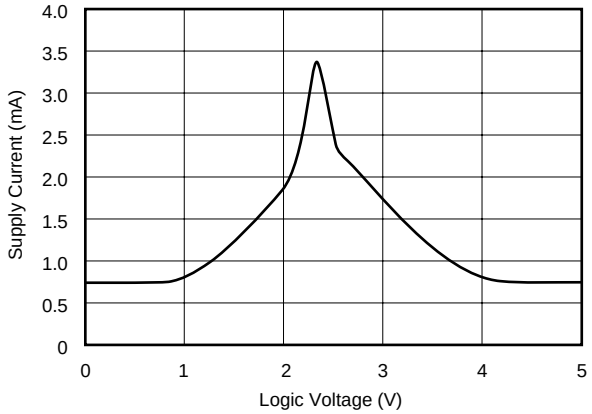
PULL-DOWN VOLTAGE vs OUTPUT SINK CURRENT



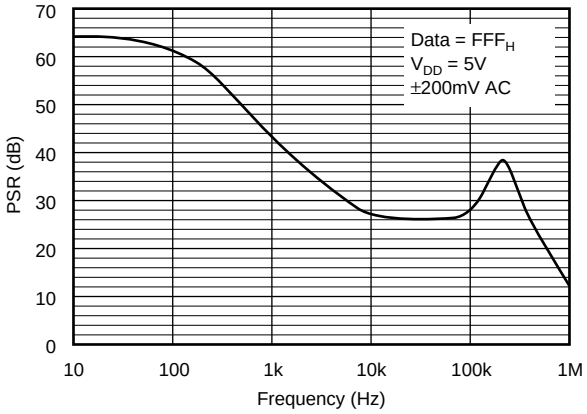
BROADBAND NOISE



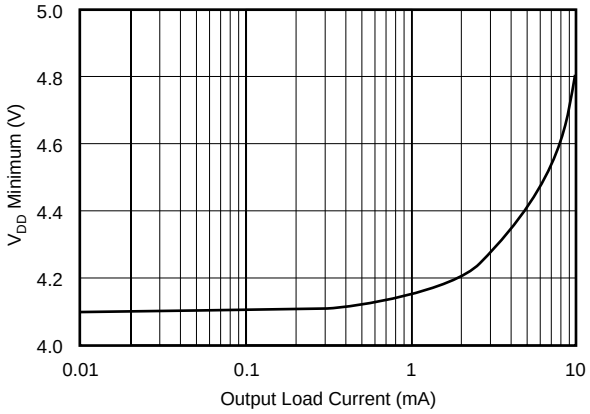
SUPPLY CURRENT vs LOGIC INPUT VOLTAGE



POWER SUPPLY REJECTION vs FREQUENCY



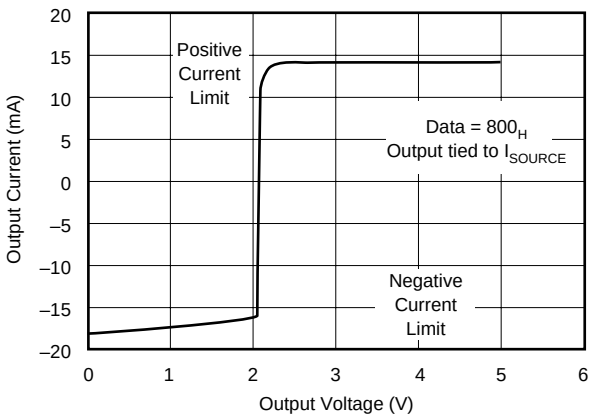
MINIMUM SUPPLY VOLTAGE vs LOAD



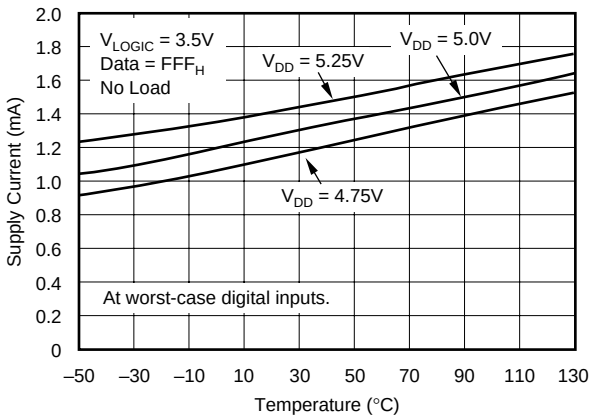
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°, and V_{DD} = 5V, unless otherwise specified.

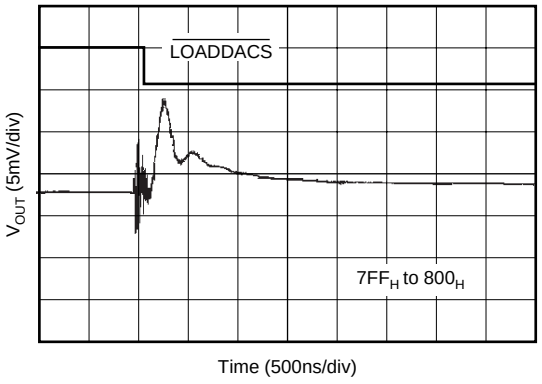
SHORT-CIRCUIT CURRENT vs OUTPUT VOLTAGE



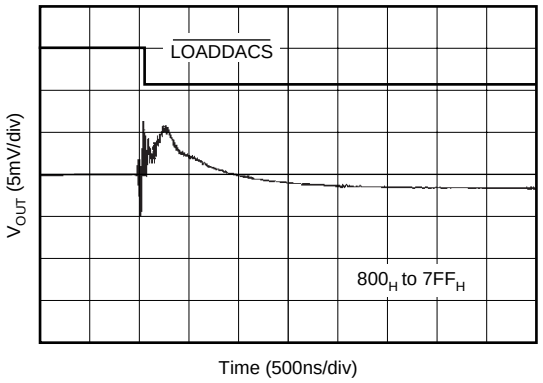
SUPPLY CURRENT vs TEMPERATURE



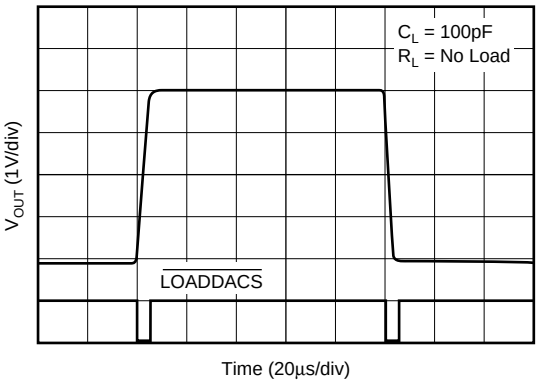
MIDSCALE GLITCH PERFORMANCE



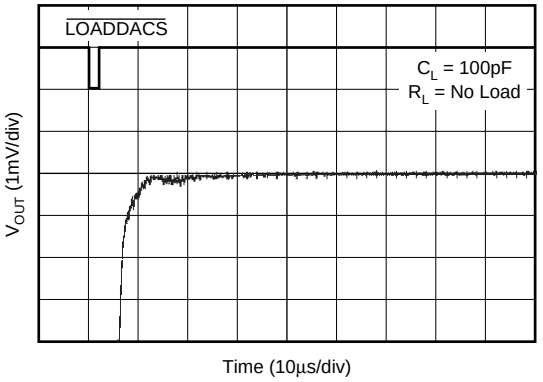
MIDSCALE GLITCH PERFORMANCE



LARGE-SIGNAL SETTLING TIME



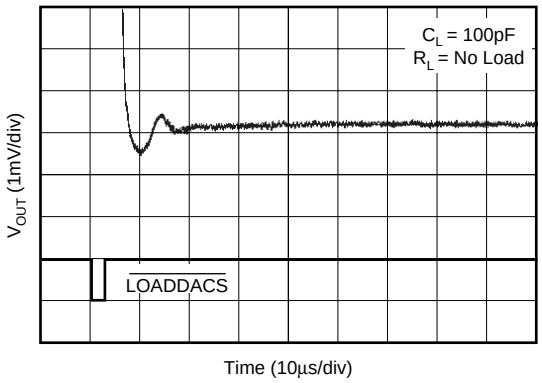
RISE TIME DETAIL



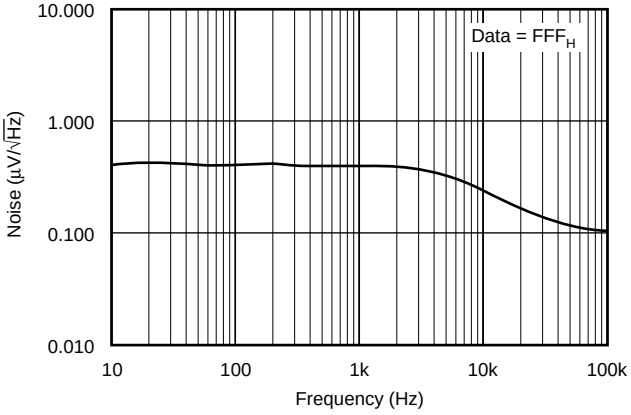
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°, and V_{DD} = 5V, unless otherwise specified.

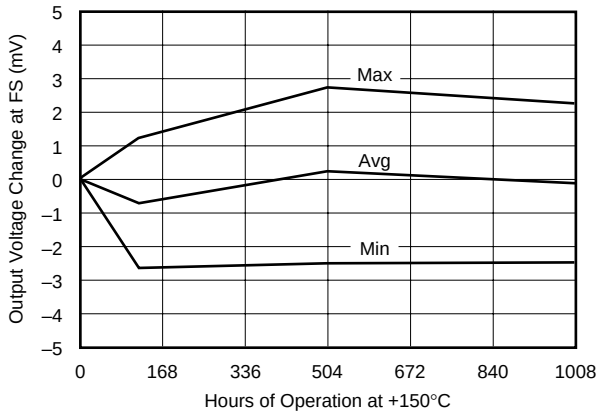
FALL TIME DETAIL



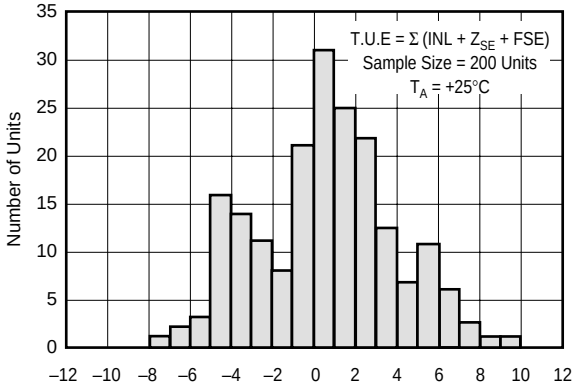
OUTPUT VOLTAGE NOISE vs FREQUENCY



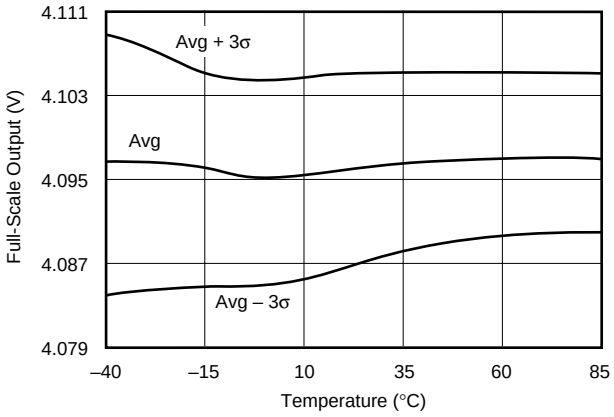
LONG-TERM DRIFT ACCELERATED BY BURN-IN



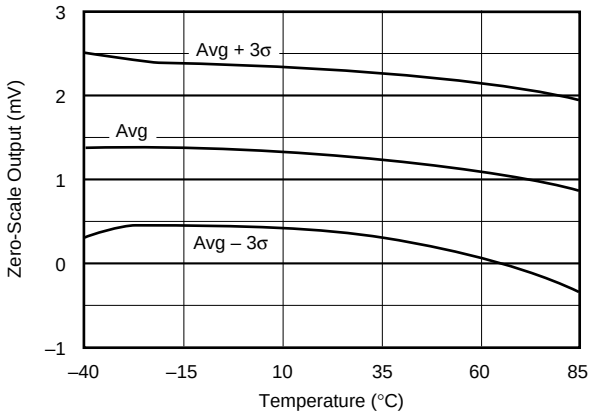
TOTAL UNADJUSTED ERROR HISTOGRAM



FULL-SCALE VOLTAGE vs TEMPERATURE



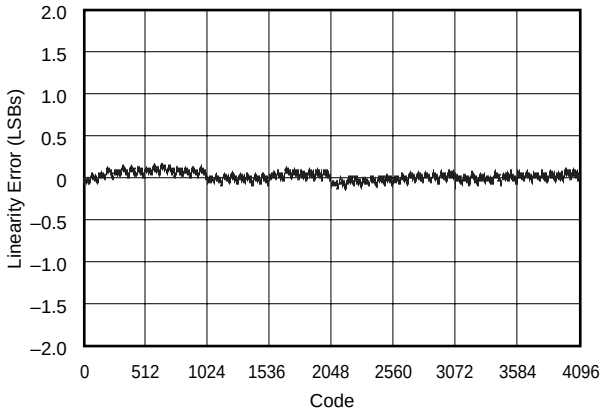
ZERO-SCALE VOLTAGE vs TEMPERATURE



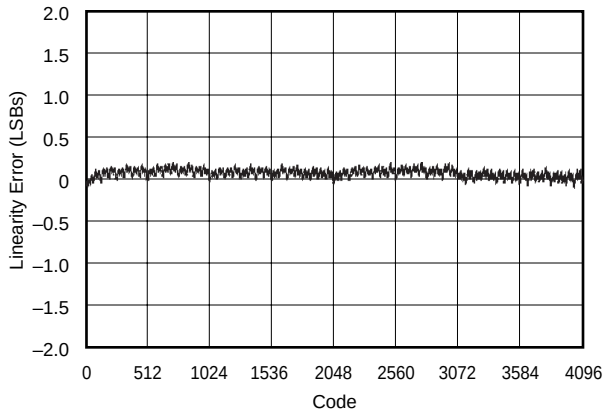
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°, and V_{DD} = 5V, unless otherwise specified.

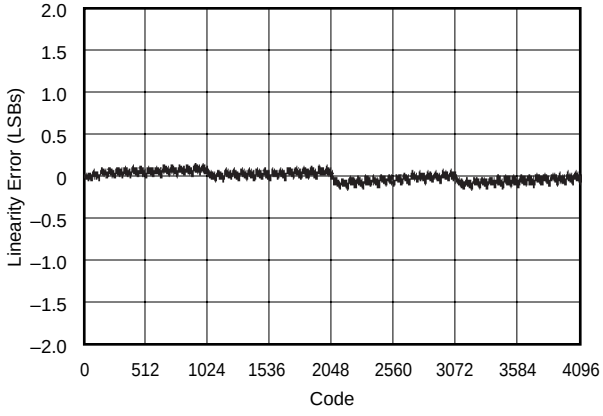
LINEARITY ERROR vs DIGITAL CODE
(DAC A at +85°C)



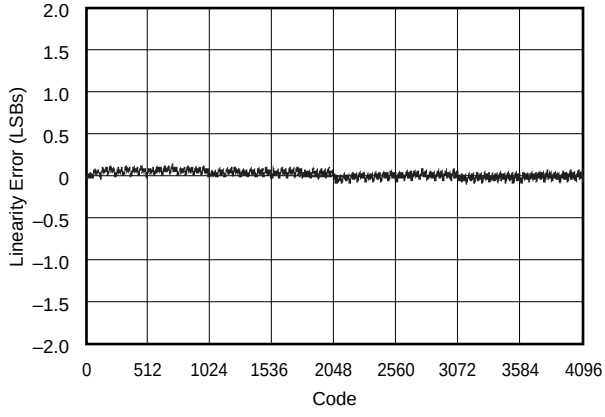
LINEARITY ERROR vs DIGITAL CODE
(DAC B at +85°C)



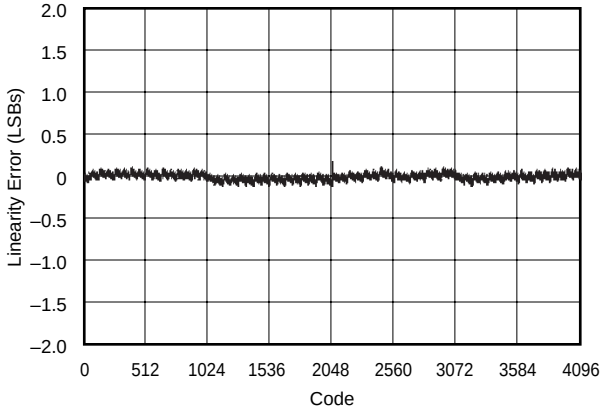
LINEARITY ERROR vs DIGITAL CODE
(DAC A at +25°C)



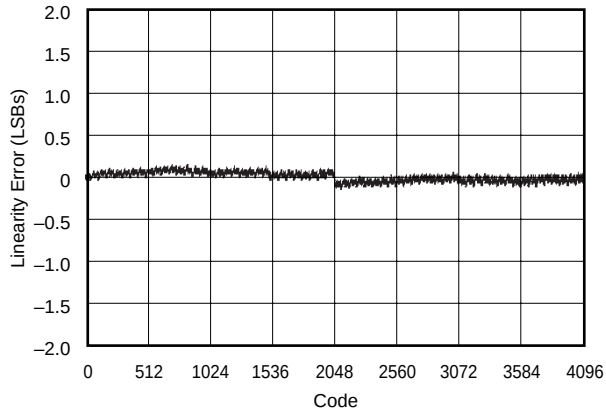
LINEARITY ERROR vs DIGITAL CODE
(DAC B at +25°C)



LINEARITY ERROR vs DIGITAL CODE
(DAC A at –40°C)



LINEARITY ERROR vs DIGITAL CODE
(DAC B at –40°C)



OPERATION

The DAC7612 is a dual, 12-bit digital-to-analog converter (DAC) complete with a serial-to-parallel shift register, DAC registers, laser-trimmed 12-bit DACs, on-board reference, and rail-to-rail output amplifiers. Figure 1 shows the basic operation of the DAC7612.

INTERFACE

Figure 1 shows the basic connection between a microcontroller and the DAC7612. The interface consists of a Serial Clock (CLK), Serial Data (SDI), and a Load DAC signal ($\overline{\text{LOADDACS}}$). In addition, a chip select ($\overline{\text{CS}}$) input is available to enable serial communication when there are multiple serial devices. Loading either DAC A or DAC B is done by shifting 14 serial bits in via the SDI input. The first 2 bits represent the address of the DAC to be updated and the next 12 bits are the code (MSB-first) sent to the DAC. The data format is Straight Binary and is loaded MSB-first into the shift registers after loading the address bits. Table I shows the relationship between input code and output voltage.

DAC7612 Full-Scale Range = 4.095V Least Significant Bit = 1mV		
DIGITAL INPUT CODE STRAIGHT OFFSETBINARY	**ANALOG OUTPUT (V)**	**DESCRIPTION**
FFF_H	+4.095	Full Scale
801_H	+2.049	Midscale + 1 LSB
800_H	+2.048	Midscale
$7FF_H$	+2.047	Midscale – 1 LSB
000_H	0	Zero Scale

TABLE I. Digital Input Code and Corresponding Ideal Analog Output.

The digital data into the DAC7612 is double-buffered. This means that new data can be entered into the chosen DAC without disturbing the old data and the analog output of the converter. At some point after the data has been entered into the serial shift register, this data can be transferred into the DAC registers. This transfer is accomplished with a HIGH to LOW transition of the $\overline{\text{LOADDACS}}$ pin. The $\overline{\text{LOADDACS}}$ pin makes the DAC registers transparent. If new data is shifted into the shift register while $\overline{\text{LOADDACS}}$ is LOW, the DAC output voltages will change as each new bit is entered. To prevent this, $\overline{\text{LOADDACS}}$ must be returned HIGH prior to shifting in new serial data.

DIGITAL-TO-ANALOG CONVERTER

The internal DAC section is a 12-bit voltage output device that swings between ground and the internal reference voltage. The DAC is realized by a laser-trimmed R-2R ladder network which is switched by N-channel MOSFETs. Each DAC output is internally connected to a rail-to-rail output operational amplifier.

OUTPUT AMPLIFIER

A precision, low-power amplifier buffers the output of each DAC section and provides additional gain to achieve a 0V to 4.095V range. Each amplifier has low offset voltage, low

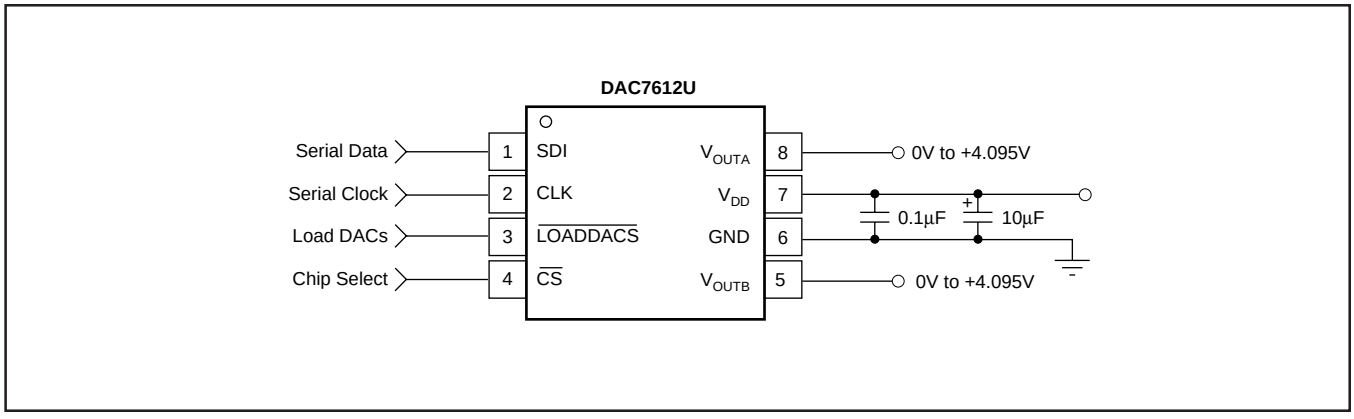


FIGURE 1. Basic Operation of the DAC7612.

noise, and a set gain of 1.682V/V (4.095/2.435). See Figure 2 for an equivalent circuit schematic of the analog portion of the DAC7612.

The output amplifier has a 7µs typical settling time to ±1 LSB of the final value. Note that there are differences in the settling time for negative-going signals versus positive-going signals.

The rail-to-rail output stage of the amplifier provides the full-scale range of 0V to 4.095V while operating on a supply voltage as low as 4.75V. In addition to its ability to drive resistive loads, the amplifier will remain stable while driving capacitive loads of up to 500pF. See Figure 3 for an equivalent circuit schematic of the amplifier's output driver and the Typical Performance Curves section for more information regarding settling time, load driving capability, and output noise.

POWER SUPPLY

A BiCMOS process and careful design of the bipolar and CMOS sections of the DAC7612 result in a very low power device. Bipolar transistors are used where tight matching and low noise are needed to achieve analog accuracy, and CMOS transistors are used for logic, switching functions and for other low power stages.

If power consumption is critical, it is important to keep the logic levels on the digital inputs (SDI, CLK, $\overline{CS}$, $\overline{LOADDACS}$) as close as possible to either V_{DD} or ground. This will keep the CMOS inputs (see "Supply Current vs Logic Input Voltages" in the Typical Performance Curves) from shunting current between V_{DD} and ground.

The DAC7612 power supply should be bypassed as shown in Figure 1. The bypass capacitors should be placed as close to the device as possible, with the 0.1µF capacitor taking priority in this regard. The "Power Supply Rejection vs Frequency" graph in the Typical Performance Curves section shows the PSRR performance of the DAC7612. This should be taken into account when using switching power supplies or DC/DC converters.

In addition to offering guaranteed performance with V_{DD} in the 4.75V to 5.25V range, the DAC7612 will operate with reduced performance down to 4.5V. Operation between 4.5V and 4.75V will result in longer settling time, reduced performance, and current sourcing capability. Consult the "V_{DD} vs Load Current" graph in the Typical Performance Curves section for more information.

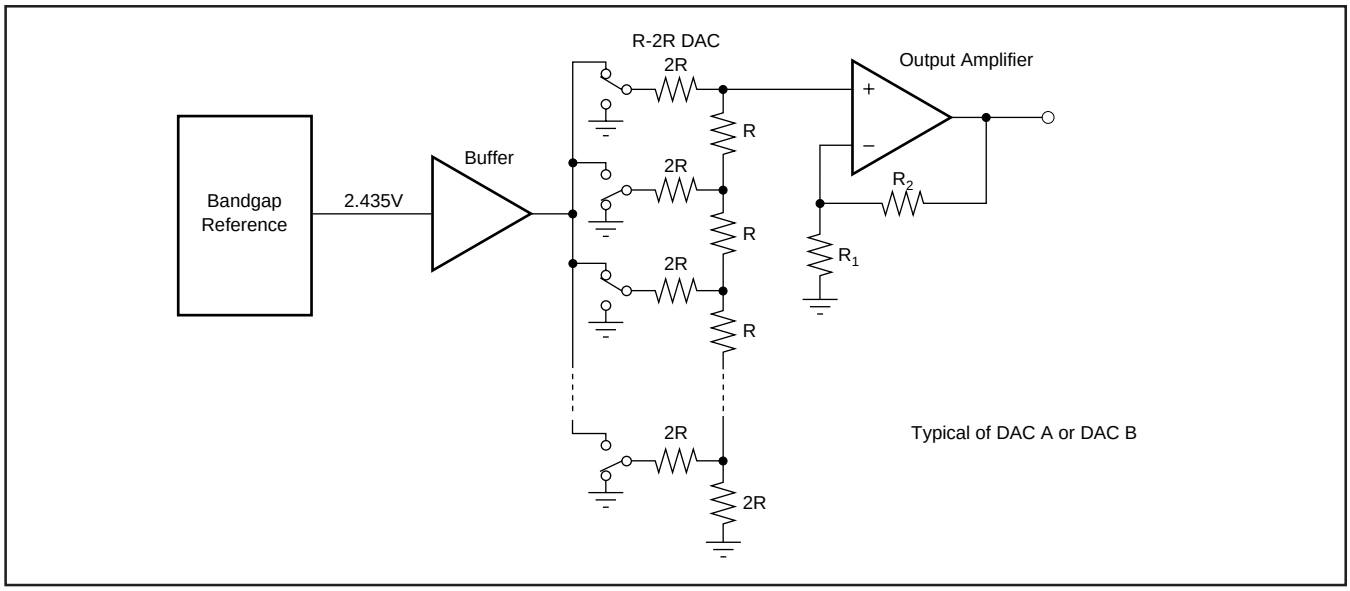


FIGURE 2. Simplified Schematic of Analog Portion.

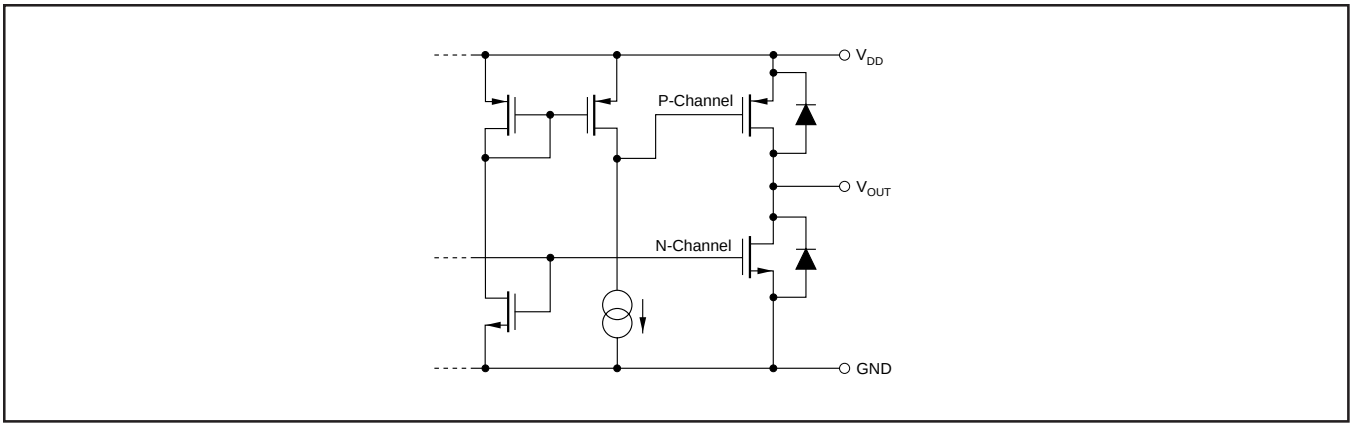


FIGURE 3. Simplified Driver Section of Output Amplifier.

APPLICATIONS

POWER AND GROUNDING

The DAC7612 can be used in a wide variety of situations—from low power, battery operated systems to large-scale industrial process control systems. In addition, some applications require better performance than others, or are particularly sensitive to one or two specific parameters. This diversity makes it difficult to define definite rules to follow concerning the power supply, bypassing, and grounding. The following discussion must be considered in relation to the desired performance and needs of the particular system.

A precision analog component requires careful layout, adequate bypassing, and a clean, well-regulated power supply. As the DAC7612 is a single-supply, +5V component, it will often be used in conjunction with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it will be to achieve good performance.

Because the DAC7612 has a single ground pin, all return currents, including digital and analog return currents, must flow through this pin. The GND pin is also the ground reference point for the internal bandgap reference. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they are connected at the power entry point of the system (see Figure 4).

The power applied to V_{DD} should be well regulated and low-noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between V_{DD} and V_{OUT}.

As with the GND connection, V_{DD} should be connected to a +5V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. In addition, the 10µF and 0.1µF capacitors shown in Figure 4 are strongly recommended and should be installed as close to V_{DD} and ground as possible. In some situations, additional bypassing may be required such as a 100µF electrolytic capacitor or even a "Pi" filter made up of inductors and capacitors—all designed to essentially lowpass filter the +5V supply, removing the high frequency noise (see Figure 4).

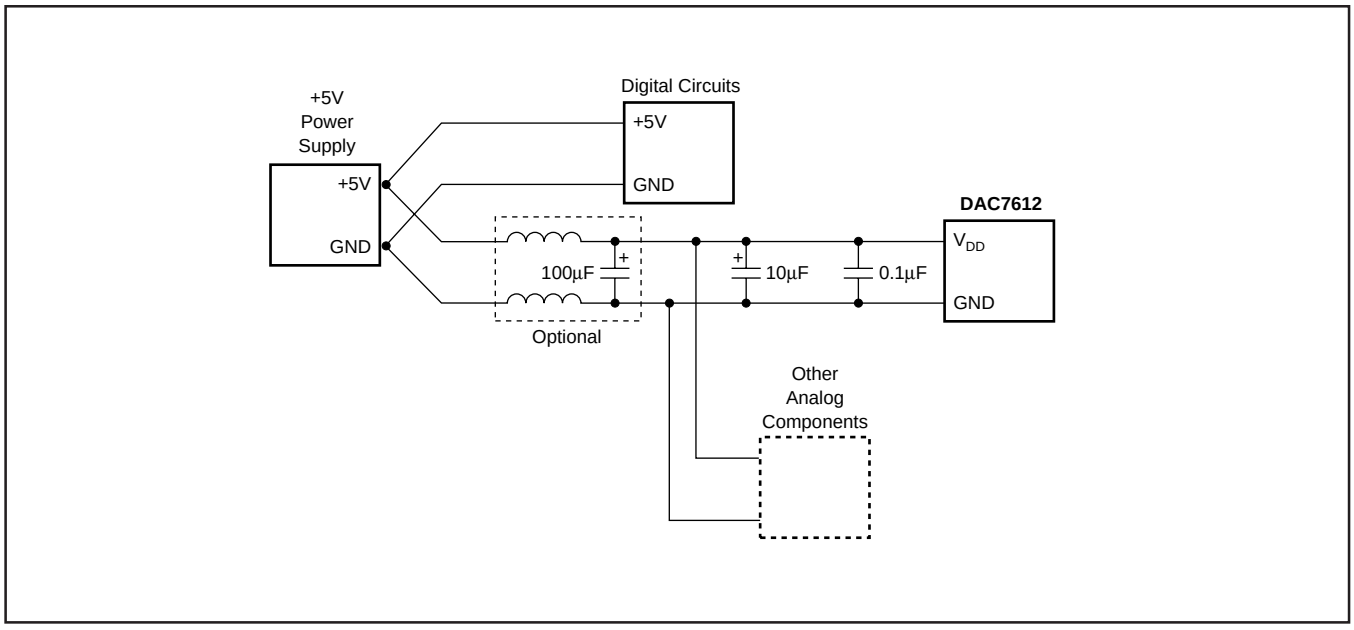


FIGURE 4. Suggested Power and Ground Connections for a DAC7612 Sharing a +5V Supply with a Digital System.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7612U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC 7612U	Samples
DAC7612U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC 7612U	Samples
DAC7612UB	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC 7612U B	Samples
DAC7612UB/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC 7612U B	Samples
DAC7612UG4	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC 7612U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

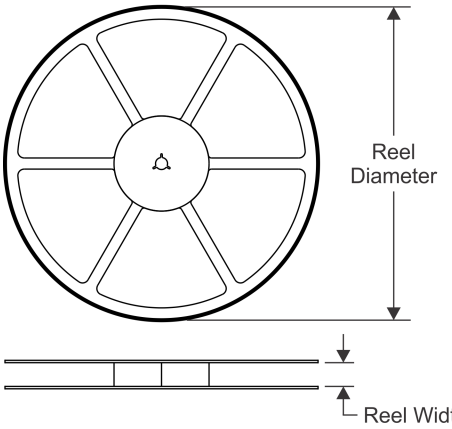
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

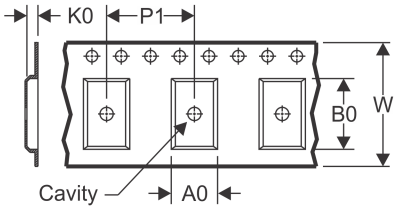
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

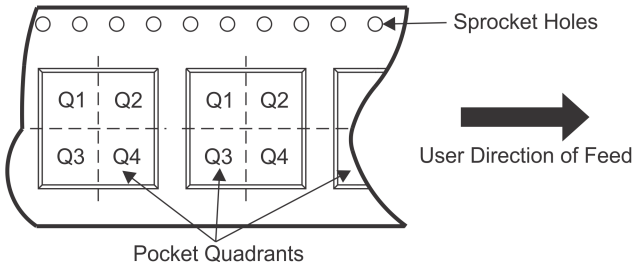


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

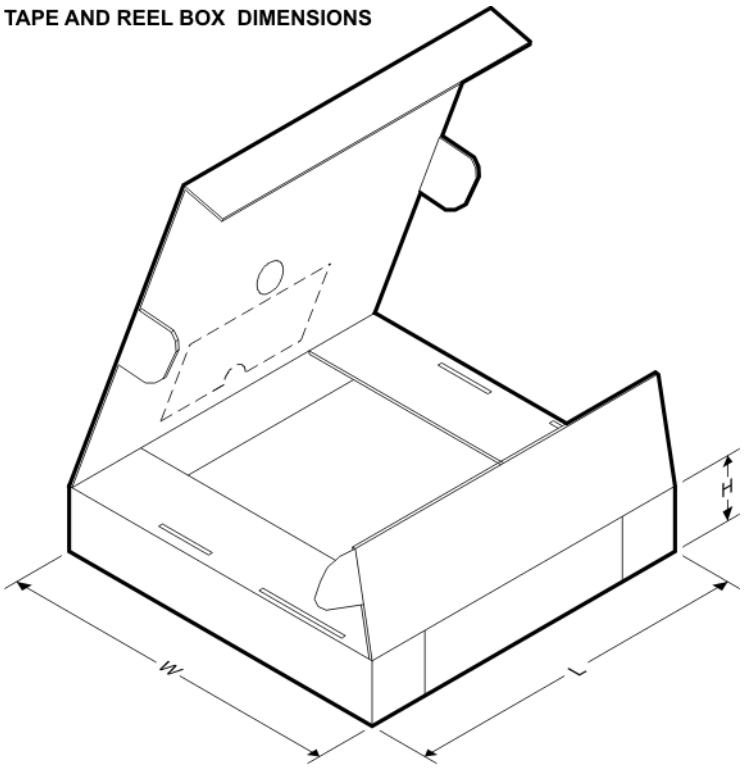
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7612U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
DAC7612UB/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

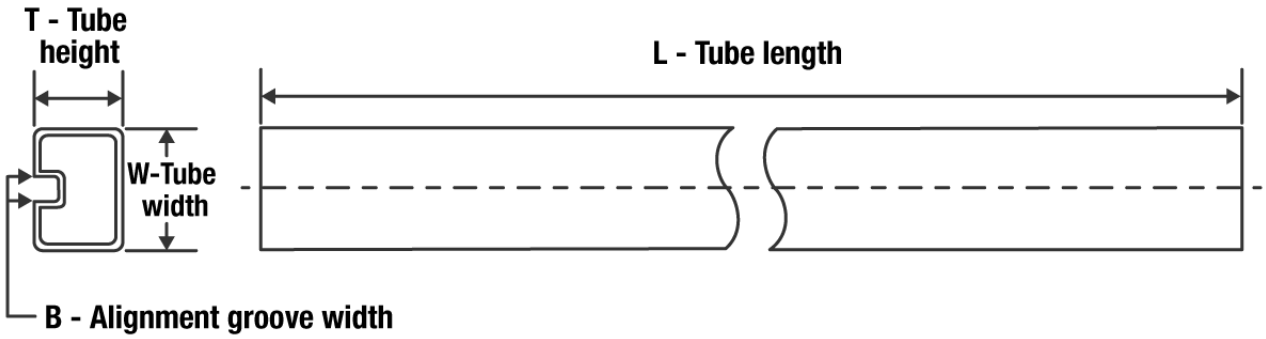
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7612U/2K5	SOIC	D	8	2500	853.0	449.0	35.0
DAC7612UB/2K5	SOIC	D	8	2500	853.0	449.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DAC7612U	D	SOIC	8	75	506.6	8	3940	4.32
DAC7612UB	D	SOIC	8	75	506.6	8	3940	4.32
DAC7612UG4	D	SOIC	8	75	506.6	8	3940	4.32

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265