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June 2014

74LVX08

Low Voltage Quad 2-Input AND Gate

Features

- Input Voltage Level Translation from 5 V to 3 V
- Ideal for Low-power / Low-Noise 3.3 V Applications
- Guaranteed Simultaneous Switching Noise Level and Dynamic threshold Performance

Description

The LVX08 contains four 2-input AND gates. The inputs tolerate voltages up to 7 V allowing the interface of 5 V systems to 3 V systems.

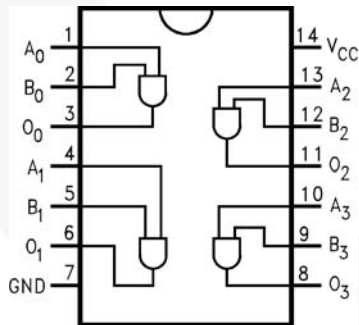
Ordering Information

| Part Number | Top Mark | Package | Packing Method | Packing Description |
|-------------|----------|-----------|----------------|---|
| 74LVX08M | LVX08 | SOIC 14L | Rail | 14-Lead Small Outline Integrated Circuit, JEDEC MS-012, 0.150 inch Narrow |
| 74LVX08MX | LVX08 | SOIC 14L | Tape and Reel | 14-Lead Small Outline Integrated Circuit, JEDEC MS-012, 0.150 inch Narrow |
| 74LVX08MTCX | LVX08 | TSSOP 14L | Tape and Reel | 14-Lead Thin Shrink Small Outline Package, JEDEC MO-153, 4.4 mm Wide |

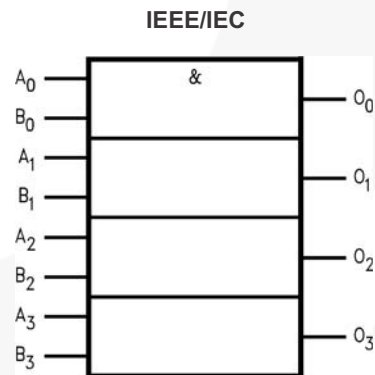


All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Logic Symbol



Pin Description

| Pin Names | Description |
|------------|-------------|
| A_n, B_n | Inputs |
| O_n | Outputs |

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating | |
|-----------------------|--|----------------------------|--------|
| V_{CC} | Supply Voltage | -0.5 V to 7.0 V | |
| I_{IK} | DC Input Diode Current, $V_I = -0.5$ V | -20 mA | |
| V_I | DC Input Voltage | -0.5 V to 7.0 V | |
| I_{OK} | DC Output Diode Current | $V_O = -0.5$ V | -20 mA |
| | | $V_O = V_{CC} + 0.5$ V | +20 mA |
| V_O | DC Output Voltage | -0.5 V to $V_{CC} + 0.5$ V | |
| I_O | DC Output Source or Sink Current | ± 25 mA | |
| I_{CC} or I_{GND} | DC V_{CC} or Ground Current | ± 50 mA | |
| T_{STG} | Storage Temperature | -65°C to 150°C | |
| P | Power Dissipation | 180 mW | |
| T_L | Lead Temperature (Soldering, 10 seconds) | 240°C | |

Recommended Operating Conditions⁽¹⁾

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Rating |
|-----------------------|--------------------------|--------------------|
| V_{CC} | Supply Voltage | 2.0 V to 3.6 V |
| V_I | Input Voltage | 0 V to 5.5 V |
| V_O | Output Voltage | 0 V to V_{CC} |
| T_A | Operating Temperature | -40°C to 85°C |
| $\Delta t / \Delta V$ | Input Rise and Fall Time | 0 ns/V to 100 ns/V |

Note:

- Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

| Symbol | Parameter | V _{CC} | Conditions | T _A = 25°C | | | T _A = -40°C to +85°C | | Unit |
|-----------------|---------------------------|-----------------|--|-----------------------|------|------|---------------------------------|------|------|
| | | | | Min. | Typ. | Max. | Min. | Max. | |
| V _{IH} | HIGH Level Input Voltage | 2.0 | | 1.5 | | | 1.5 | | V |
| | | 3.0 | | 2.0 | | | 2.0 | | |
| | | 3.6 | | 2.4 | | | 2.4 | | |
| V _{IL} | LOW Level Input Voltage | 2.0 | | | | 0.5 | | 0.5 | V |
| | | 3.0 | | | | 0.8 | | 0.8 | |
| | | 3.6 | | | | 0.8 | | 0.8 | |
| V _{OH} | HIGH Level Output Voltage | 2.0 | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -50 μA | 1.9 | 2.0 | | 1.9 | | V |
| | | 3.0 | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -50 μA | 2.9 | 3.0 | | 2.9 | | |
| | | | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -4 mA | 2.58 | | | 2.48 | | |
| V _{OL} | LOW Level Output Voltage | 2.0 | V _{IN} = V _{IL} or V _{IH} , I _{OL} = -50 μA | | 0.0 | 0.1 | | 0.1 | V |
| | | 3.0 | V _{IN} = V _{IL} or V _{IH} , I _{OL} = -50 μA | | 0.0 | 0.1 | | 0.1 | |
| | | | V _{IN} = V _{IL} or V _{IH} , I _{OL} = -4 mA | | | 0.36 | | 0.44 | |
| I _{IN} | Input Leakage Current | 3.6 | V _{IN} = 5.5 V or GND | | | ±0.1 | | ±1.0 | μA |
| I _{CC} | Quiescent Supply Current | 3.6 | V _{IN} = V _{CC} or GND | | | 2.0 | | 20.0 | μA |

Noise Characteristics⁽²⁾

| Symbol | Parameter | V _{CC} (V) | C _L (pF) | T _A = 25°C | | Unit |
|------------------|--|---------------------|---------------------|-----------------------|-------|------|
| | | | | Typ. | Limit | |
| V _{OLP} | Quiet Output Maximum Dynamic V _{OL} | 3.3 | 50 | 0.3 | 0.5 | V |
| V _{OLV} | Quiet Output Minimum Dynamic V _{OL} | 3.3 | 50 | -0.3 | -0.5 | V |
| V _{IHD} | Minimum HIGH Level Dynamic Input Voltage | 3.3 | 50 | | 2.0 | V |
| V _{ILD} | Maximum LOW Level Dynamic Input Voltage | 3.3 | 50 | | 0.8 | V |

Note:2. Input t_r = t_f = 3 ns

AC Electrical Characteristics

| Symbol | Parameter | V _{CC} (V) | C _L (pF) | T _A = 25°C | | | T _A = -40°C to +85°C | | Unit |
|--|--------------------------------------|---------------------|---------------------|-----------------------|------|------|---------------------------------|------|------|
| | | | | Min. | Typ. | Max. | Min. | Max. | |
| t _{PLH} , t _{PHL} | Propagation Delay Time | 2.7 | 15 | | 6.3 | 11.4 | 1.0 | 13.5 | ns |
| | | | 50 | | 8.8 | 14.9 | 1.0 | 17.0 | |
| | | 3.3 ± 0.3 | 15 | | 4.8 | 7.1 | 1.0 | 8.5 | |
| | | | 50 | | 7.3 | 10.6 | 1.0 | 12.0 | |
| t _{OSLH} , t _{OSHL} | Output to Output Skew ⁽³⁾ | 2.7 | 50 | | | 1.5 | | 1.5 | ns |
| | | 3.3 | | | | 1.5 | | 1.5 | |

Note:

3. Parameter guaranteed by design $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.

Capacitance

| Symbol | Parameter | T _A = 25°C | | | T _A = -40°C to +85°C | | Unit |
|-----------------|--|-----------------------|------|------|---------------------------------|------|------|
| | | Min. | Typ. | Max. | Min. | Max. | |
| C _{IN} | Input Capacitance | | 4 | 10 | | 10 | pF |
| C _{PD} | Power Dissipation Capacitance ⁽⁴⁾ | | 18 | | | | pF |

Note:

4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

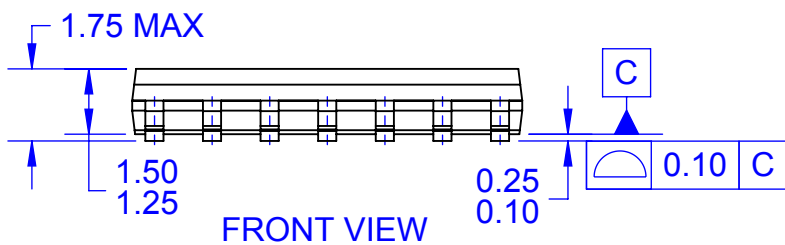
Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} \times I_{CC}}{4 \text{ (per Gate)}}$



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 2009.
- E. LANDPATTERN STANDARD: SOP65P640X110-14M.
- F. DRAWING FILE NAME: MKT-MTC14rev7.





NOTES:

- A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
- D. LAND PATTERN STANDARD: SOIC127P600X145-14M
- E. CONFORMS TO ASME Y14.5M, 2009
- D. DRAWING FILENAME: MKT-M14Arev14



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